Effect of RFI on the Error Probabilities of Synchronizer Circuits

Kam-Wing Li, *Member, IEEE*, Safwat G. Zaky, and Keith G. Balmain, *Life Fellow, IEEE*

***Abstract*—This paper examines the ways in which radio frequency interference (RFI) affects the error probability of synchronizer circuits. Two effects are predicted analytically and demonstrated experimentally. In one case, RFI changes the effective sampling time of the synchronizer output. In the second, RFI affects the nonlinear input–output pulsewidth transfer characteristic of a logic chain causing the pulsewidth distribution at the synchronizer input to be modified. It is shown that RFI may increase or decrease the error probability of a synchronizer circuit depending on circuit parameters and on the point of injection of the RFI.**

***Index Terms*—Electromagnetic interference, metastability, radio frequency interference, reliability, synchronizer failure.**

I. Introduction

THE reliability of a logic circuit in an electromagnetic environment depends on how logic elements react to interference. Earlier investigations of the effects of radio frequency interference (RFI) on logic elements centered around simple logic gates such as NAND gates [1], [2], and usually dealt with logic failures arising from RFI-induced changes in logic levels. Tront [3] first identified two types of upsets, which were later called static and dynamic upsets by Laurin [4]. Static upsets are those involving a change in the logic level of a signal, while dynamic upsets involve a change in the timing of a logic transition. In the case of a logic gate, upsets are temporary; that is, the gate's output returns to its normal value once the interference is removed. On the other hand, RFI coupled to a flip-flop may cause a permanent change in state. Such effects have been examined empirically by Kenneally [5].

Flip-flops are used extensively for synchronizing asynchronous logic signals, which arise when a synchronous digital system interacts with the outside world or with another digital system having a different timing reference. In such applications, the flip-flops are usually referred to as synchronizers. There is always a nonzero error probability associated with a synchronizer circuit, because of the possibility of a flip-flop entering the metastable state [6]. Similar errors arise in arbiter circuits, which are used to choose between two asynchronous requests. It has been shown that the delays associated with metastability place an upper limit on the performance of asynchronous circuits [7]. Various aspects of metastability and the accompanying failures in flip-flops have been the subject of investigation by many researchers [8]–[14]. Because of its significant effect on the reliability of high-speed digital systems, metastability continues to be an important topic of research.

This paper examines two RFI-induced effects in logic gates that may affect the failure rate of a synchronizer circuit. The effect of interference-induced changes in propagation delay on the error probability is investigated first. Next, a new phenomenon is described involving the input pulses to the synchronizer. It is shown that the pulsewidth distribution at the input of a synchronizer may be modified by the interference signal, and hence may lead to a change in the probability of the synchronizer element entering the metastable state.

Although the discussion in the paper refers to synchronizer circuits, most of the observations made are equally applicable to arbiter circuits. The main difference is that some of the signal configurations encountered in synchronizers may not arise in arbiters.

The study is limited to the case of single-frequency (CW) interference. Also, the ways in which RFI is generated or coupled to the circuit are not discussed. To simplify the analysis, only single-node RFI injection is considered. We begin by giving a simple model for the synchronizer circuit during recovery from metastability.

II. A Typical Synchronizer Circuit

A typical synchronizer circuit is shown in Fig. 1. The circuit has two inputs—one for the reference clock and the other for an asynchronous data stream. The output of the synchronizer is sampled by a third signal, the sampling clock. The synchronizer element is separated from the output and the two inputs by logic gates, which represent the propagation delays that inevitably exist in any circuit implementation.

The purpose of the synchronizer circuit is to determine the state of the asynchronous input at a particular instant relative to the reference clock. Let $t = t_0$ be the time at which the active edge of the reference clock is applied to the input of the circuit in Fig. 1. After some delay, the clock edge reaches point Q and causes the synchronizer element to test the state of point P and produce a corresponding output at point R, which in turn propagates to point V. The signal at point V reaches its steady-state value at time t_r, as shown in part (b)

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K.-W. Li was with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, Ont., Canada M5S 3G4. He is now with Northern Telecom, Ottawa, Ont., Canada K2C 0A7.

S. G. Zaky and K. G. Balmain are with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, Ont., Canada M5S 3G4 (e-mail: safwat@eecg.utoronto.ca).

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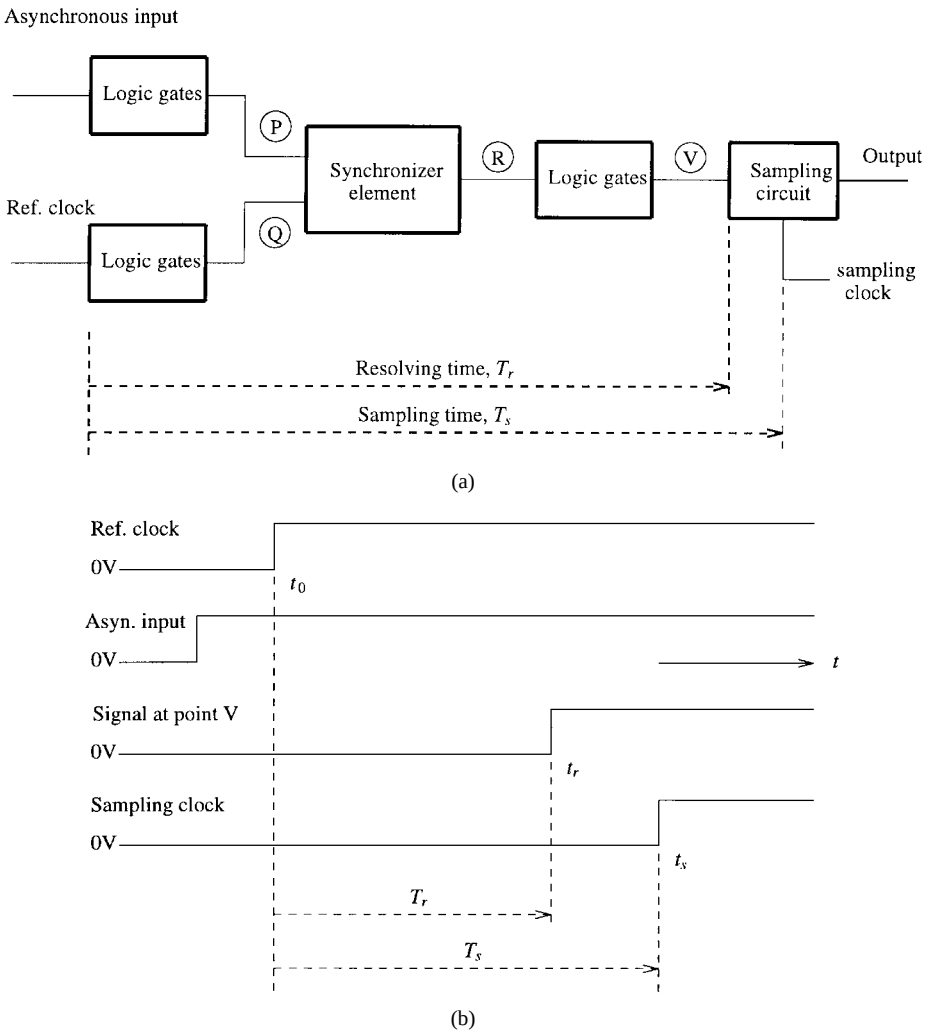

Fig. 1. Timing of the operation of a synchronizer circuit.

of the figure. The active edge of the sampling clock, which occurs at time t_s, represents the time at which the rest of the system uses the information at point V. Clearly, for the system to operate correctly, we must have $t_s > t_r$. We will refer to $T_r = t_r - t_0$ and $T_s = t_s - t_0$ as the resolving time and the sampling time of the synchronizer circuit, respectively.

When the signal transitions at points P and Q are far apart, no metastability arises. We will call the resolving time in this case the normal propagation delay T_p; that is, in the absence of metastability, $T_r = T_p$. When the transitions at points P and Q are sufficiently close to each other, the synchronizer element enters the metastable state and an additional delay T_m is encounted before steady state is reached. Thus, in general, $T_r = T_p + T_m$.

A circuit that implements the synchronizer element in Fig. 1 is shown in Fig. 2. When the signals at points P and Q are combined at point S, they result in a pulse of width w_i equal to the time separation of the two signals. The resolving time T_r of the synchronizer increases indefinitely as w_i approaches a critical pulsewidth value w_c. We are interested in a small range of pulsewidth around $w_i = w_c$ within which the resolving time T_r of the synchronizer circuit exceeds the sampling time T_s, thus leading to synchronization failure. Since $T_r = T_p + T_m$, failure occurs when $T_m \geq T_s - T_p$. The right-hand side of this inequality is the effective sampling time of the circuit after accounting for the normal propagation delay. It has been shown that if a synchronizer element enters the metastable state as a result of an input pulse of width w_i, the recovery time T_m is such that [8]

$$|w_i - w_c| = Ce^{-G_B T_m}$$

where C and G_B are constants determined by the circuit parameters of the synchronizer element. Therefore, the range of pulsewidth for which $T_m \geq T_s - T_p$ is given by

$$w_c - \Delta w \leq w_i \leq w_c + \Delta w$$

where Δw is a function of the sampling time of the form

$$\Delta w = Ce^{-G_B(T_s - T_p)}. \tag{1}$$

In the lower half of this range, $w_c - \Delta w \leq w_i < w_c$, the synchronizer's output after recovery from the metastable state reaches one of its two stable states, which we will call 0. In the other half of the range, the synchronizer recovers to the 1 state. For a given circuit configuration, only one of these conditions is likely to lead to errors. We will assume, without

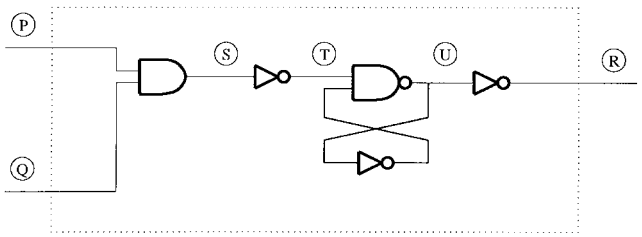

Fig. 2. A possible arrangement of the synchronizer block in Fig. 1.

loss of generality, that synchronization errors occur only in the interval $w_c \le w_i \le w_c + \Delta w$, which we will refer to as the *critical window* of the synchronizer. The corresponding width Δw of this window is referred to as the *critical window width* of the synchronizer.

Let $f(w_i)$ be the probability density function (pdf) of the input pulsewidth. Hence, the probability of error for each input data transition is given by

$$P(\text{error}) = \int_{w_c}^{w_c+\Delta w} f(w_i)\, dw_i. \tag{2}$$

The usual way of describing the performance of a synchronizer circuit is in terms of the mean time between failures (MTBF), which is inversely proportional to the probability of error. For asynchronous data, the timing separation between the reference clock and the input data can have any value between 0 and the clock period, and all values are equally probable; that is,

$$f(w_i) = \begin{cases} f_c, & \text{for } 0 \le w_i \le \dfrac{1}{f_c} \\ 0, & \text{otherwise} \end{cases} \tag{3}$$

where f_c is the clock frequency. Therefore, for f_D data transitions per second, we obtain [10]

$$\text{MTBF} = \frac{1}{f_D f_c \Delta w}. \tag{4}$$

Note that the mathematical model leading to (1)–(4) was derived with reference to the synchronizer circuit in Fig. 2. However, this model is applicable to any synchronizer circuit that has the general structure shown in Fig. 1.

In the remainder of this paper, we examine the effect of RFI injected at nodes P, Q, or R in Fig. 1. According to (2), RFI will change the probability of error if it affects the critical window width Δw, or if it changes the distribution of the input pulsewidth described by $f(w_i)$. In Section III, we examine the effect of interference on the sampling time, T_s, which determines Δw according to (1). The effect on input pulsewidth distribution is discussed in Section IV.

III. Effect of RFI-Induced Delay

When RFI is injected at a node, it changes the propagation delay through the logic gates connected to that node [4], [15]. An interference signal applied to node P will change the timing of individual data events. However, it will not affect the statistical distribution of the timing separation between data and clock transitions, and hence it should not affect the failure rate of the synchronizer. On the other hand, the change in propagation delay caused by interference injected at node Q or node R will change the effective sampling time of the synchronizer. Let T_d be the RFI-induced delay, which should be added to the normal propagation delay T_p of the synchronizer. The effective sampling time of the circuit becomes $T_s - T_p - T_d$, and failure will occur when $T_m \ge T_s - T_p - T_d$. Equation (1) now becomes

$$\Delta w_d = Ce^{-G_B(T_s - T_p - T_d)}$$

where Δw_d is the critical window width in the presence of the interference signal.

It has been shown in [4] and [15] that low-level RFI introduces a change in delay that varies linearly with the interference level, that is,

$$T_d = pv_a$$

where p is a constant, and v_a is the instantaneous interference voltage level at the time the transition occurs. Thus,

$$\begin{aligned} \Delta w_d &= Ce^{-G_B(T_s - T_p - pv_a)} \\ &= \Delta w_0 e^{\beta v_a} \end{aligned} \tag{5}$$

where Δw_0 is the critical window width with no induced delay, and $\beta = pG_B$. Since v_a can either be positive or negative, T_d can have a positive or a negative value, leading to either an increase or a decrease in Δw_d, respectively.

Equation (5) shows that the width of the critical window is a function of the induced interference voltage v_a, which is a function of time. The average critical window width in the presence of interference can now be obtained by computing the expected value of Δw_d, as follows:

$$E[\Delta w_d] = \int \Delta w_d f(v_a)\, dv_a \tag{6}$$

where $f(v_a)$ is the probability density function of v_a, and the integration is carried over all possible values of v_a. In the case of a sine wave with a peak voltage V_p, $f(v_a)$ is given by

$$f(v_a) = \frac{1}{\pi\sqrt{V_p^2 - v_a^2}}.$$

Substituting from (5) into (6) we obtain

$$E[\Delta w_d] = \Delta w_0 \int_{-V_p}^{V_p} \frac{e^{\beta v_a}}{\pi\sqrt{V_p^2 - v_a^2}}\, dv_a. \tag{7}$$

The equation above allows a quantitative prediction of the RFI effect [16]. Also, the integral on the right-hand side can be shown to be greater than one, which means that RFI-induced delay will lead to an increase in the average critical window width. This observation has been confirmed experimentally, as described below.

A. Experimental Results

A CMOS edge-triggered D flip-flop (74C74) was used to build the synchronizer circuit shown in Fig. 3. The experimental setup, which is described in the Appendix, enabled the timing separation between the input data transition and the rising edge of the clock to be adjusted and the resolving time

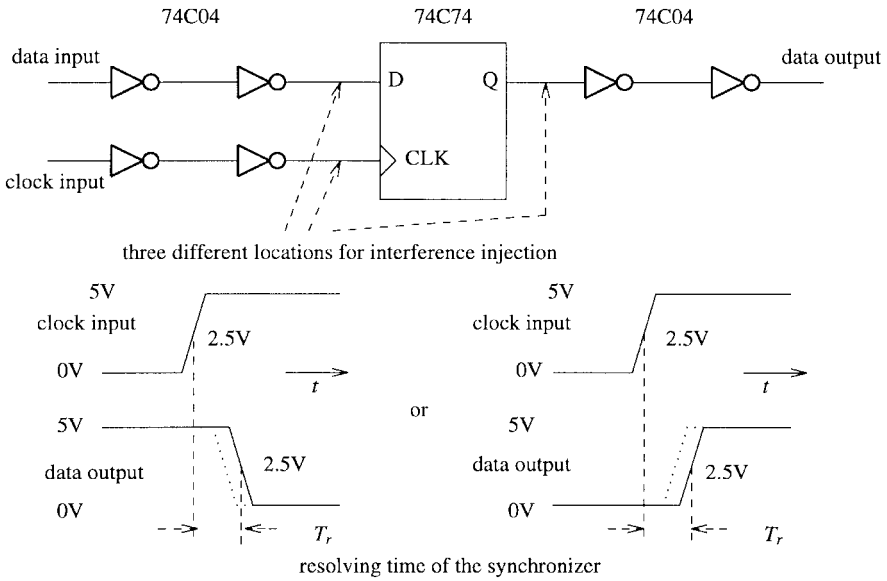

Fig. 3. A D-flip-flop synchronizer circuit and the associated resolving time.

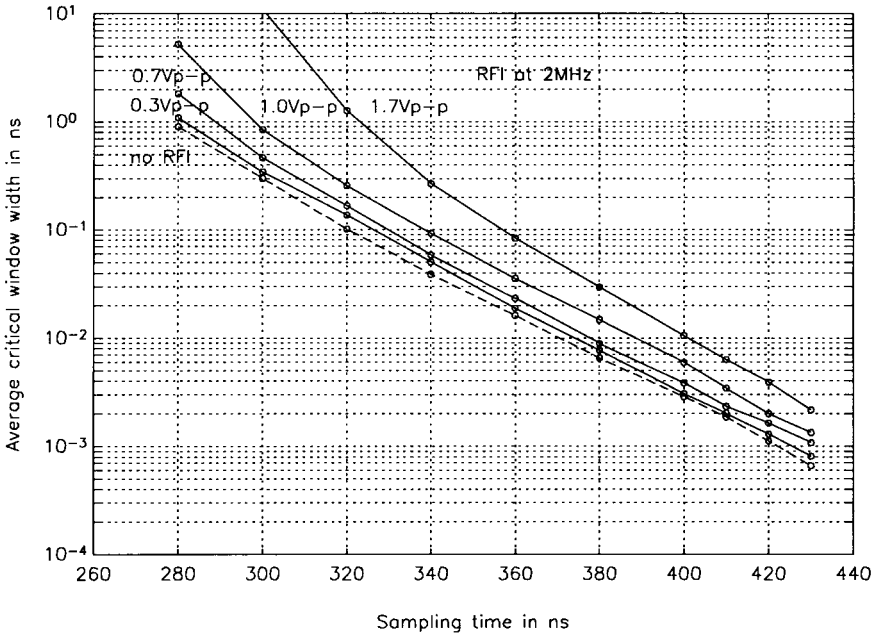

Fig. 4. Effect of RFI injected at node Q of the synchronizer circuit of Fig. 3 on the average critical window width of the circuit.

T_r of the synchronizer circuit to be measured. The resolving time was measured between the 2.5 V crossings, as shown in Fig. 3. For a given value of the sampling time T_s, a probability curve for $T_r > T_s$ was obtained as described in the appendix, and the average width of the critical window Δw_d was derived by determining the area under the probability curve. The experiment was repeated for different values of T_s, and the results are shown in Fig. 4.

The dotted line in Fig. 4 gives the average value of Δw for negative data transitions as a function of the sampling time T_s in the absence of interference. The relationship is very close to being linear on a semilogarithmic scale, as predicted by (1). The solid curves were obtained with a 2-MHz interference signal injected at the Q output of the flip-flop. They give the average critical window width $E[\Delta w_d]$ associated with negative data transitions at Q for different interference signal levels. Clearly, the critical window width increases with the interference level. Similar results were obtained for positive transitions as well as when the interference signal was injected at the clock input of the flip-flop. However, RFI injected at input D had little effect on the critical window width.

These results are in agreement with the analysis given at the beginning of this section in conjunction with the circuit of Fig. 2. The D input of the flip-flop in Fig. 3 is equivalent to node P in Fig. 2. Interference injected at this node changes the timing of individual events, but not their statistical distribution. Hence, it has no effect on the critical window width. On the other hand, the clock input and the Q

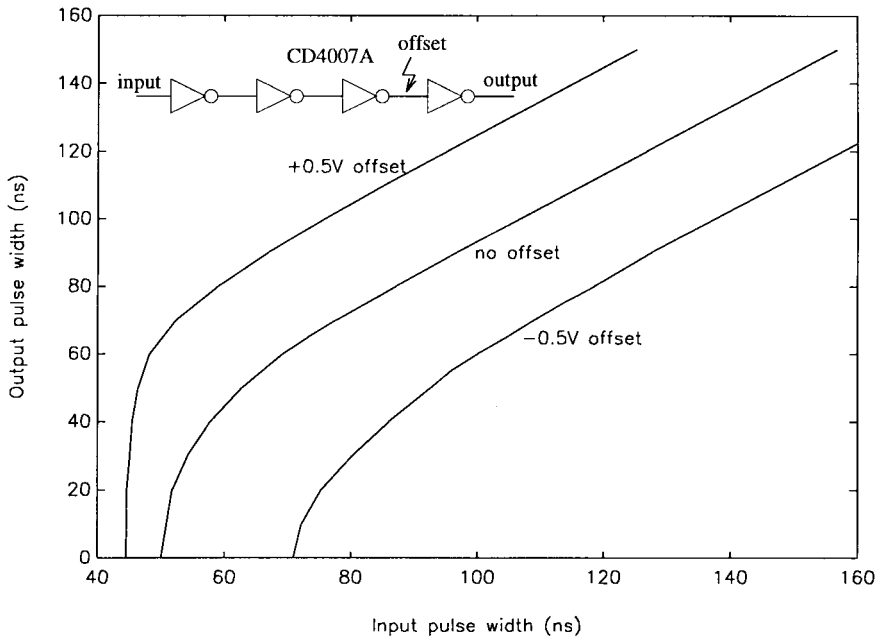

Fig. 5. Effect of voltage offset on pulsewidth.

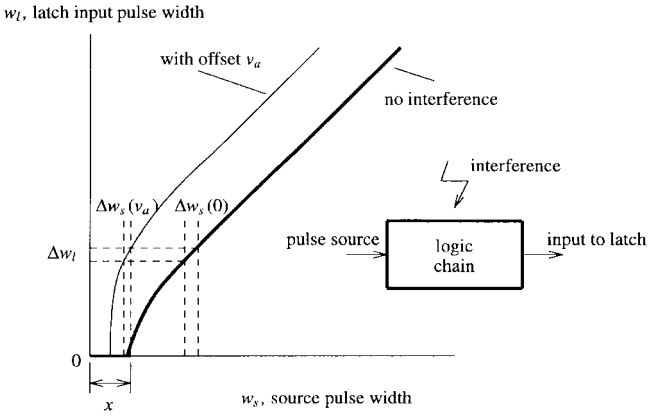

Fig. 6. Input–output pulsewidth relationship for a chain of logic gates.

output in Fig. 3 are equivalent to nodes Q and R, respectively, in Fig. 2. Interference injected at either of these nodes affects the sampling time, and hence the width of the critical window.

IV. Effect of Change in Pulsewidth Distribution

The RFI-induced change in propagation delay is not the same for the rising and falling edges of a logic signal. As a result, a logic signal in the form of a pulse may experience a change in pulsewidth in the presence of RFI. This effect is illustrated in Fig. 5, which gives the output pulsewidth as a function of the input pulsewidth as measured experimentally for the chain of four CMOS inverters shown in the inset. The "no offset" curve gives the results in the absence of interference. The lower and upper curves correspond to the cases where the instantaneous value of the interference signal causes the pulse to be shifted by −0.5 V and +0.5 V, respectively, at the input of the last inverter.

Each of the three curves consists of two regions—a linear region and a nonlinear region. The linear region occurs at wide input pulsewidths, and has a slope of one. In this region, any change in pulsewidth at the input results in an equal change in pulsewidth at the output. In the nonlinear region, where the slope is larger than one, a small change in input pulsewidth results in a larger change at the output. We will call this the "small signal" pulsewidth expansion effect, in analogy with the small signal voltage gain of a voltage amplifier. To avoid cumbersome terminology, the modifier "small signal" will be dropped in subsequent discussion. It should be regarded as implied wherever the term pulsewidth expansion is used.

Fig. 5 shows that an offset caused by interference changes the slope and width of the nonlinear region, hence the associated amount of pulsewidth expansion. Furthermore, the effect is not symmetrical for positive and negative offsets. Since the range of pulsewidths that leads to metastability in synchronizer operation normally lies in the nonlinear region, RFI injected at the input of a synchronizer can change the pulsewidth distribution and, as a result, the effective width of the critical window. We will show that this is in fact the case.

Consider again the synchronizer circuit in Fig. 2. The pulses produced by combining the two input signals are fed to the latch through a chain of logic gates. Let Δw_l be the critical window width at the input of the latch. The corresponding range of pulsewidth at the input to the logic chain is Δw_s, which may be smaller than Δw_l because of pulsewidth expansion as pulses travel through the gates. Furthermore, a voltage offset v_a caused by RFI injected near the input of the latch may change the amount of pulsewidth expansion, hence the value of Δw_s, as illustrated in Fig. 6. For input pulses whose width is in the nonlinear region of the transfer characteristic, $\Delta w_s(v_a) < \Delta w_s(0)$ for $v_a > 0$.

Consider now the case of a low-frequency CW interference signal, where positive and negative offsets occur with equal probability. The period of the CW signal is assumed to be sufficiently larger than the critical window width that

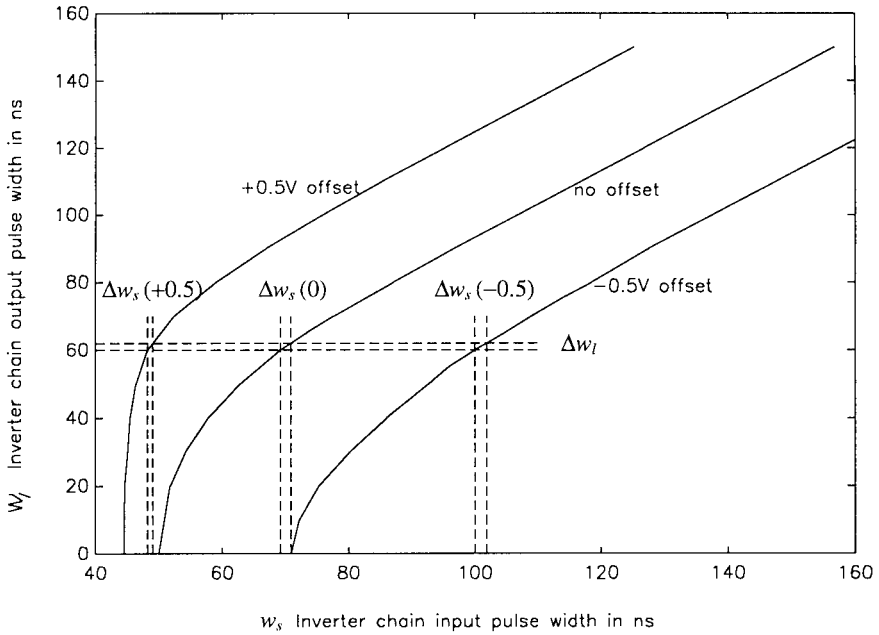

Fig. 7. Relation between the critical window widths at the input (horizontal axis) and output (vertical axis) of the inverter chain of Fig. 5 for various interference voltage levels. The average window width with symmetrical offsets is smaller than that with no offset.

interference around the critical window can be represented by a dc offset voltage. Fig. 7 shows the values of Δw_s for $v_a = \pm 0.5$ V. It can be easily seen from this figure that the average of the two values $\Delta w_s(+0.5)$ and $\Delta w_s(-0.5)$ is smaller than or equal to $\Delta w_s(0)$. Thus, for any interference waveform that is symmetrical around zero, the expected value of Δw_s satisfies the relation

$$E[\Delta w_s(v_a)] \leq \Delta w_s(0).$$

The reduction in the effective window width at the pulse source means that interference will reduce the failure rate of the synchronizer.

The effect of interference can also be understood by examining the probability density function (pdf) of the pulsewidth at different points in the circuit. The pulsewidth at the source is uniform, as given by (3), and is illustrated in Fig. 8(a). The pdf of the pulsewidth at the latch input can be derived from the distribution in Fig. 8(a) and transfer characteristics similar to those in Fig. 5, for all possible values of offset. After averaging, we obtain the pdf curves in Fig. 8(b). The probability of error is given by (2), and is equal to the area under the pdf curve within the critical window Δw_l. Fig. 8 shows that this area is reduced in the presence of interference.

The effect of high-frequency interference has not been included in the work reported in this paper. It should be pointed out that Laurin's results [4] show that high-frequency signals have little effect on signal timing, because the input stage of a chip acts as a low-pass filter.

A. Experimental Results

In order to evaluate the effect of RFI-induced pulsewidth expansion on the probability of error of a synchronizer, the circuit shown in Fig. 9 was built and tested. Pulses are fed to the input of a latch from a pulse source through an inverter

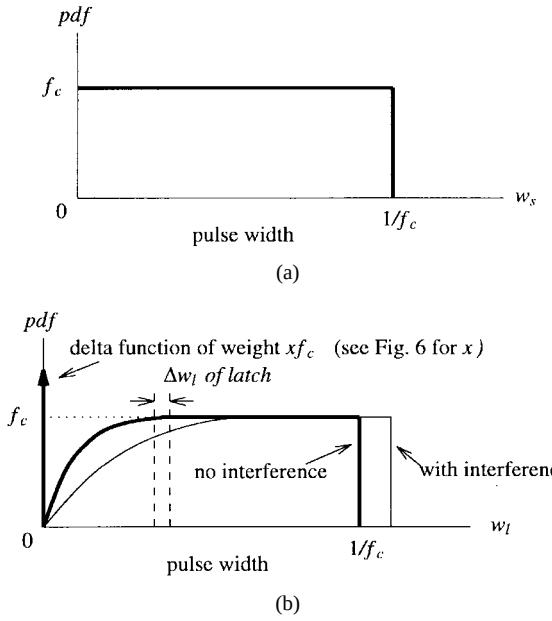

Fig. 8. Effects of pulsewidth expansion on the pdf of the pulsewidth.

chain, and the output of the latch is sampled by a sampling circuit as before. A narrow pulse that reaches node T will cause a sampling error if its width w_i is within the critical window, that is, if $w_c \leq w_i \leq w_c + \Delta w_l$.

The interference signal is fed at point S in the middle of the chain, representing the case of a synchronizer in which RFI affects the input pulses directly, causing pulsewidth modulation. The discussion above suggests that this may lead to a reduction in the error rate of the synchronizer.

The effect of pulsewidth modulation on the error rate cannot be measured in isolation, because an RFI signal injected at point S will also cause a change in the effective sampling

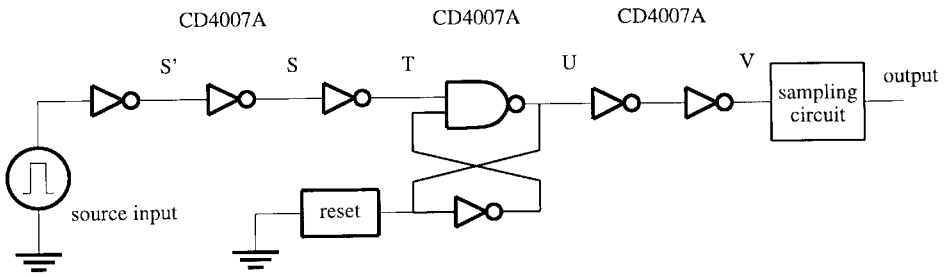

Fig. 9. A latch circuit fed from a pulse source through an inverter chain.

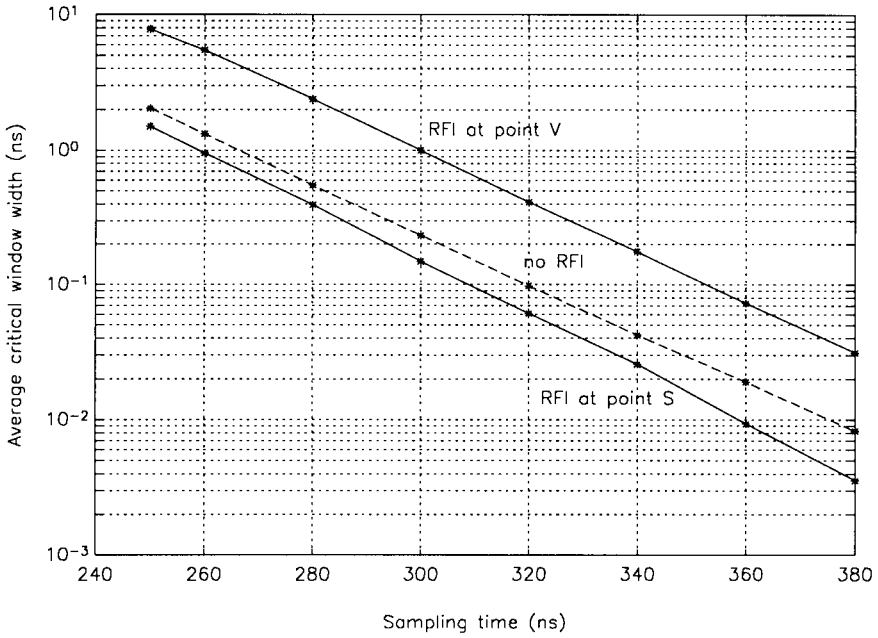

Fig. 10. Experimental results showing the effect of an RFI signal of 1.5 Vp-p at 2 MHz.

time as explained in Section III. To evaluate the effect of pulsewidth modulation, two sets of experimental results were obtained, which are given in Fig. 10. First, RFI was injected at point V. Since no narrow pulses exist at this point, only the effect of RFI on the sampling time is present, and, as in the case of Fig. 4, RFI causes an increase in the average width of the critical window. The experiment was then repeated with RFI injected at point S, where it will affect both the sampling time and the pulsewidth. As is clearly seen in the figure, the combined effect leads to a reduction in the average width of the critical window, showing that at least in this particular case the RFI-induced pulsewidth expansion effect is dominant.

The amount of RFI-induced pulsewidth expansion changes with the length of the inverter chain and the location of RFI injection [16]. When RFI was injected at point S' instead of point S in Fig. 9, the critical window width was almost the same as for no RFI. This means that the contributions from induced pulsewidth expansion and induced delay were almost equal and opposite, and more or less cancelled one another.

V. Conclusions

It has been shown both by analysis and by measurement that RFI in a synchronizer circuit can affect the synchronization error probability in two ways. When RFI is injected between the reference clock and the circuit that samples the synchronizer's output, the resulting changes in propagation delay affect the time available for recovery from the metastable state. For CW interference, this effect leads to an increase in the error probability. When the interference signal is injected near the synchronizer's input, it may also cause a change in the probability distribution of the narrow pulses that cause the synchronizer to enter the metastable state. On average, this effect leads to a reduction in the effective width of the critical window, and thus reduces the probability of error.

The above results show that electromagnetic interference can have a significant effect on the behavior of synchronizer circuits. These effects should be taken into account in the design of synchronizer circuits to minimize the induced delay, and in their physical layout to control RFI coupling.

Appendix
Average Critical Window Width Measurements

The experimental setup for measuring the average critical window widths described in Section III is shown in Fig. 11. The same setup with the appropriate circuit-under-test was also used in Section IV. All the instruments are connected via the GPIB interface bus, and measurements are controlled by software in the host computer.

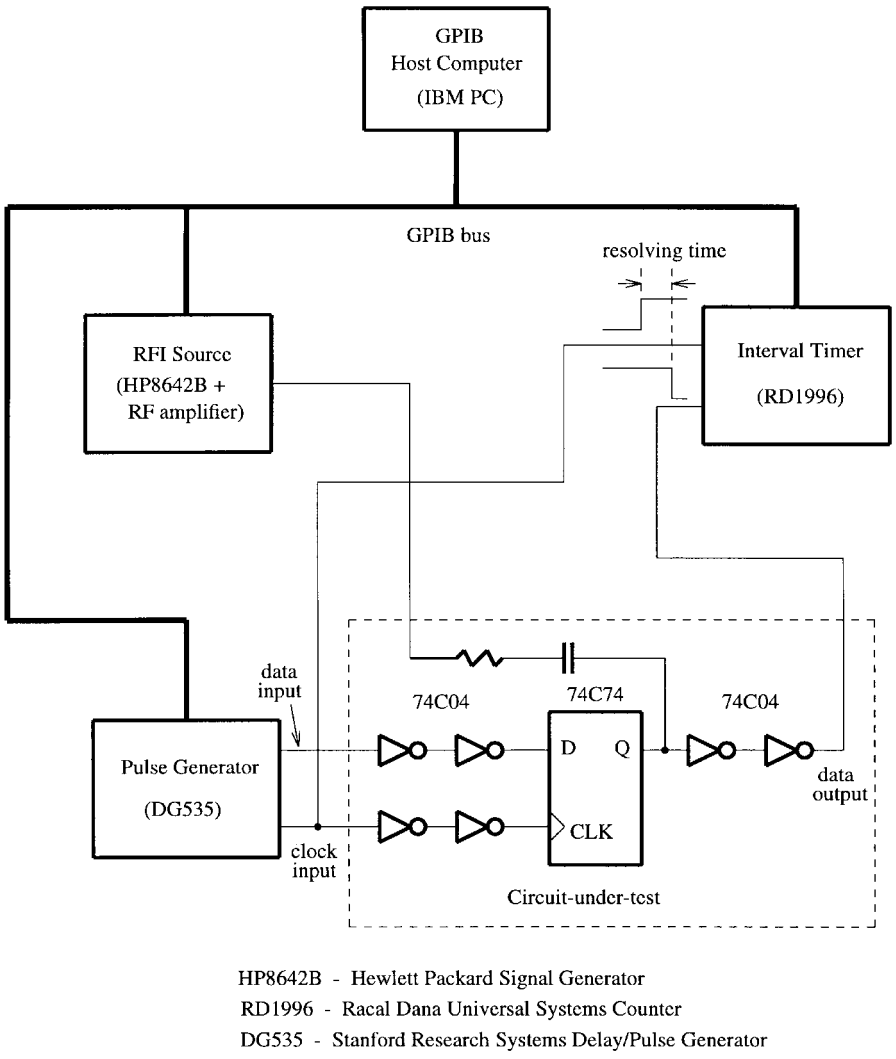

Fig. 11. Test setup for determining the synchronizer circuit resolving time and the associated critical window width.

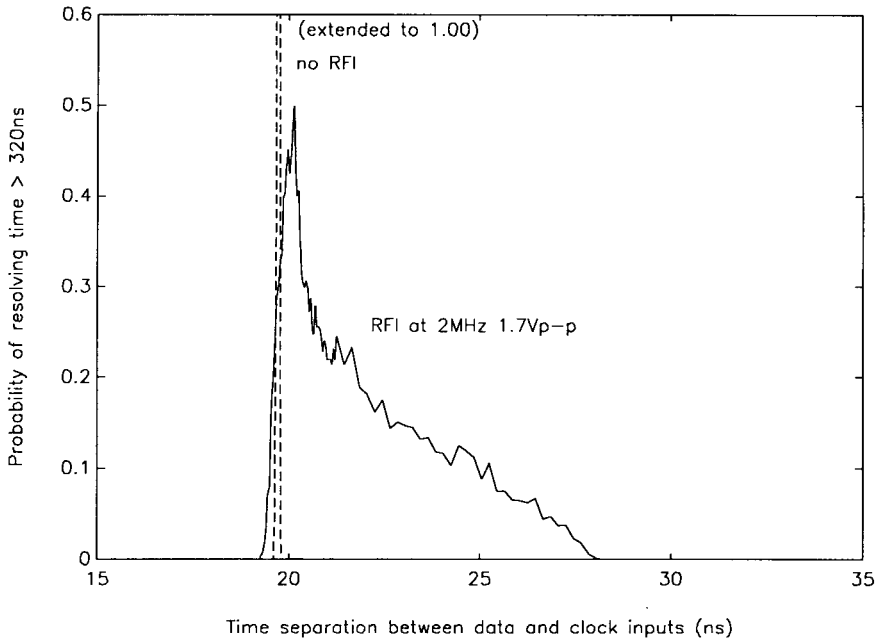

Fig. 12. Critical window distribution for a sampling time of 320 ns for the synchronizer circuit-under-test shown in Fig. 11.

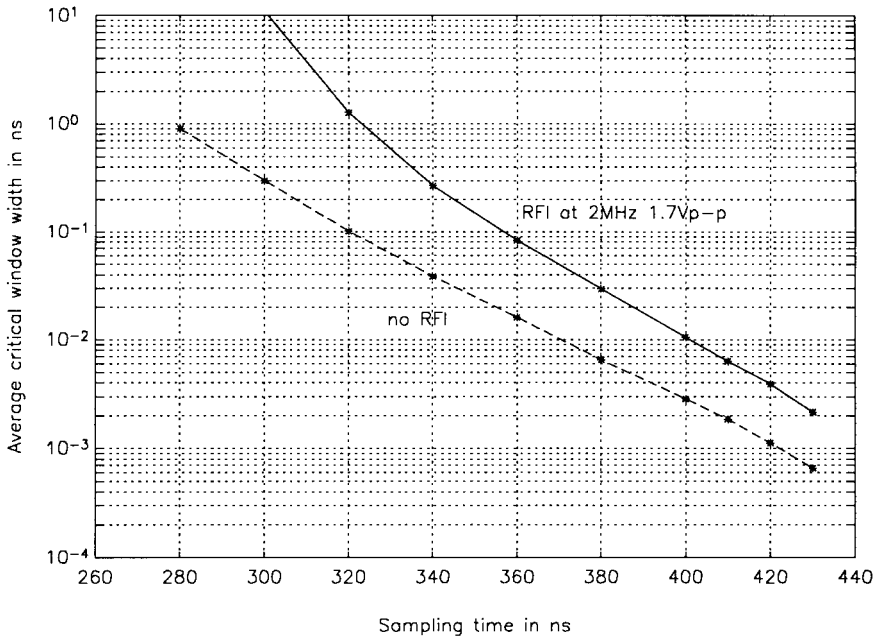

Fig. 13. The critical window width versus the sampling time characteristic of the synchronizer circuit-under-test shown in Fig. 11.

Measurement procedures were as follows. A CW interference source of a certain amplitude and frequency was injected at the circuit node of interest, and two synchronized pulse trains with adjustable time separation were applied to the data and the clock inputs of the circuit. The pulses were uncorrelated with the interfering signal. Depending on the timing of the data with respect to the clock signal, a logic transition may or may not occur at the output after the active clock edge. Whenever a transition occurred, the resolving time of the output data relative to the active (rising) edge of the reference clock was measured by the Interval Timer.

Rough measurements were taken beforehand to determine the approximate range of time separations between the data and clock signals that gave rise to a large resolving time. Then, the range was divided into 50 or more time separations which were arranged in a pseudorandom sequence. A pseudorandom sequence was used to reduce the effect of drift in the circuit under test, and the measurements were repeated 1000 times to obtain the failure probability distribution. For each time separation, the resolving times were compared to a given sampling time value T_s to determine the percentage of readings that exceeded T_s. This procedure was repeated for other time separations, and a probability curve similar to that shown in Fig. 12 was obtained. There are two curves in the figure, the solid curve corresponds to a 2-MHz, 1.7-Vp-p interference signal, and a sampling time of 320 ns. The dashed curve corresponds to no interference. Different probability curves were obtained for different sampling times.

The error probability of a synchronizer circuit is proportional to the area under the probability curve. This area has a unit of time, and is equal to the average critical window width of the synchronizer circuit for a particular sampling time. Hence, a plot of the average critical window width versus the sampling time can be obtained as shown in Fig. 13.

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Kam-Wing Li (S'93–M'95) received the Master of Applied Science degree and Ph.D. degree in electrical and computer engineering from the University of Toronto in 1992 and 1996, respectively.

He currently works as an ASIC designer at Nortel in Ottawa, Canada.

Safwat G. Zaky received the B.Sc. degree in electrical engineering and the B.Sc. degree in mathematics, both from Cairo University, Egypt, and the M.A.Sc. and Ph.D. degrees in electrical engineering from the University of Toronto.

He is a Professor in the Department of Electrical and Computer Engineering, University of Toronto, where he is currently Department Chair. He is also a Professor in the Department of Computer Science. His current research interests are in the areas of computer architecture, logic synthesis and electromagnetic compatibility of digital systems. Prior to joining the University of Toronto, he was with Bell Northern Research, Bramalea, Ont., Canada, where he worked on applications of electrooptics and magnetics in mass storage and telephone switching. He was a senior visitor with the Computer Laboratory, University of Cambridge, England, in 1980/1981. He has coauthored two books, *Computer Organization* and *Microcomputer Structures*.

Dr. Zaky is a member of the Association of Professional Engineers of Ontario.

Keith G. Balmain (S'56–M'63–SM'85–F'87–LF'97) was born in London, Ont., Canada, on August 7, 1933. He received the B.A.Sc. degree in engineering physics from the University of Toronto, Toronto, Ont., Canada, in 1957, and the M.S. and Ph.D. degrees in electrical engineering from the University of Illinois, Urbana, in 1959 and 1963, respectively.

He was an Assistant Professor of Electrical Engineering at the University of Illinois, associated primarily with the Aeronomy Laboratory, until 1966. He then joined what is now the Department of Electrical and Computer Engineering, at the University of Toronto, where he is a Professor and holds the NSERC/Bell Canada/Nortel Industrial Research Chair in Electromagnetics. He was Chairman of the Division of Engineering Science for two-and-a-half years until 1987, after which he chaired the University of Toronto's Research Board for a three-year term. His research has focused on antennas in plasma, broadband antennas, radio wave scattering from power lines and high-rise buildings, electrostatic charge accumulation and arc discharges on both spacecraft and human subjects, and electromagnetic compatibility.

Dr. Balmain was corecipient of the IEEE Antennas and Propagation Society Best Paper of the Year Award in 1970, and in 1992 was corecipient of a NASA Group Achievement Award related to electrical grounding on the Space Station. He coauthored the second edition of *Electromagnetic Waves and Radiating Systems*. His activities include membership on the IEEE Antenna Standards Committee, and Chairman of the Subcommittee on Antennas in Physical Media (1968–1976), Canadian Chairman of the International Union of Radio Science Commission IV (1970–1973), member IEEE APS AdCom (1973–1976), Associate Editor of *Radio Science* (1978–1980), and Chairman of the Technical Program Committee for the 1980 IEEE APS International Symposium held in Quebec City. Currently, he chairs the Organizing Committee for the 1999 URSI General Assembly to be held in Toronto.