Physics-Based CAD Models for the Analysis of Vias in Parallel-Plate Environments

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***Abstract*—In this paper, physics-based computer-aided-design (CAD) models for through and buried vias in parallel-plate environments are presented based on radial transmission-line theory. The crosstalk power transferred by the TEM parallel-plate mode between vias is characterized, and extended to the treatment of vias in finite substrates by means of image theory. The presented CAD models can be combined with lumped and distributed circuit elements, as well as linear and nonlinear devices, providing an accurate and fast procedure for the global modeling of high-speed electronic circuits. The corresponding simulation time for representative single or multiple via configurations has been drastically reduced compared to full-wave simulations while maintaining comparable accuracy.**

***Index Terms*—Decoupling capacitors, ground bounce, package resonances, parallel-plate noise, radial transmission lines, switching noise, vias.**

I. Introduction

IN MULTILAYER printed circuit boards and three-dimensional (3-D) packages, vias may penetrate through the conductor planes or be buried in between them. In such configurations, the loading effect of the via discontinuity to the signal line is not only the generation of conducted noise (reflections), but also the coupling of useful signal energy to the substrate. This phenomenon takes place when a time varying or a transient (switching) current flows through the via, therefore, exciting the parallel-plate mode. This effect is manifested by voltage fluctuations on the reference voltage planes, often referred to as (power/ground) noise. With the currently increasing frequency content of signals in analog and digital circuits along with the reduction of the supply voltages, this noise becomes one of the significant performance limiting factors.

Much research has focused on modeling and analyzing the parallel-plate noise excited by vias. In general, these studies can be classified into the following four categories:

1) *full-wave methods*: derivation of the Green's function of a resonant cavity to model the finite substrate and subsequent derivation of the port impedances [1] or direct 3-D numerical solution of Maxwell's equations using frequency- or time-domain full-wave techniques such as the finite-element method (FEM) and transmission-line method (TLM) [2], [3];
2) *circuit-oriented methods*: modeling the parallel plates with two-dimensional (2-D) *LC* ladder networks and analyzing them by means of a transient circuit simulator [3];
3) *analytical methods*: solution of Maxwell's equation for the dominant mode ($\mathrm{TEM}/\mathrm{TM}_{00}$) of a radial waveguide and derivation of the pertinent transfer and driving point impedances [4]–[7];
4) *hybrid methods*: combining full-wave simulations, analytical solution, or measurement results with circuit simulations either through a dynamic interaction between full-wave and circuit simulators [7] or by *processing* the data obtained from full-wave analysis, analytical solution, or measurements to extract circuit models and perform subsequent simulations [8]–[10].

In this paper, a combination of the second and third approaches has been utilized to develop computer-aided-design (CAD) models for vias embedded in parallel-plate environments. These models benefit from the accuracy and speed of an analytical approach, as well as the simplicity and versatility of a circuit-oriented approach. Specifically, based on radial transmission-line theory, physics-based models are proposed and verified for treating through and buried vias in single and multiple configurations in a multilayer parallel-plate environment. The concept of utilizing radial transmission-line theory to represent vias in a parallel-plate environment has been proposed before in [4], [5], and [7] and has been recently applied for the treatment of ball-grid array packages [6]. In a more recent work by the authors, lumped-element models for multiple buried and through vias in parallel-plate environments, including the coupling to the parallel-plate noise and package resonances, have been developed [11], [12]. In this paper, the theory behind the developed models in [11] and [12] is discussed in detail and additional models for different applications such as single and multiple through vias in stacked parallel-plate environments are presented. Furthermore, a systematic approach for utilizing more than one decoupling capacitors for noise cancellation is presented. In all cases, the models are verified against finite-difference time-domain (FDTD) numerical simulations or time-domain reflectometry (TDR) measurements.

The distinct advantages of the proposed models compared to previously reported techniques in the literature can be summarized as follows:

1) they are portable to commercial circuit simulators such as Agilent-ADS;
2) the model for the parallel plates is a one-dimensional (1-D) circuit, which drastically reduces the simulation time;

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3) the simulations are accurate since the models are physics-based;
4) the interactive coupling between the signal lines and the parallel plates is included in the models, which allows for the global simulation of the entire circuit, as well as the prediction of the noise pattern on the parallel plates;
5) the reflection from the edges in finite-size substrates can be included using a circuit-based approach;
6) different types of vias such as buried, blind, and through can be treated.

The organization of this paper is as follows. In Section II, the analytical derivation used in developing the proposed models is outlined. This part, along with Appendix B, elaborates on the definition of the coupling coefficient used in the models to include the interaction between the via and the parallel-plate mode. In Section III, equivalent circuits for different structures with infinite and finite substrates, containing single and multiple buried or through vias, are implemented in Agilent-ADS. All models are first validated against available data in the literature and then compared with FDTD simulations. Section IV contains the result of TDR measurements on representative test structures implemented to further investigate the practicality of the presented models. In addition, using the developed models, the values and locations of decoupling capacitors used for suppressing the parallel-plate noise are determined.

II. Analysis

In order to incorporate the coupling to the parallel-plate modes for vias in a parallel-plate environment using a circuit-oriented approach, the commonly used Π model of a via should be appropriately modified. The corresponding loss of useful energy and the associated signal-integrity effects become more significant as the frequency increases. For the currently available technologies, in terms of substrate and interconnect dimensions as well as the frequency spectra of the signals, almost all of the coupled energy is transferred to the dominant TEM mode. This mode propagates as a cylindrical wave [7], [11], [12], which, therefore, justifies modeling of the parallel plates using radial transmission-line theory.

A. Formulation for Modeling the Parallel Plates

For the analysis of radial waveguides, a transmission-line-type formalism can be introduced for the dominant propagating mode by solving Helmholtz' equation in cylindrical coordinates. Such a rigorous analysis yields TE^z and TM^z Hankel-type modal functions of which the TM^z_{00} (TEM) mode can be assumed as the fundamental mode [13]–[15]. The transverse modal fields for the dominant mode are defined using voltage and current representations defined by

$$\vec{E}_t(\rho, \phi, z) = \frac{V(\rho)}{h}\,\vec{a_z} \tag{1a}$$

$$\vec{H}_t(\rho, \phi, z) = \frac{I(\rho)}{2\pi\rho}\,\vec{a_z} \tag{1b}$$

where h is the height of the parallel plates and the subscript t designates transverse-field components. This definition implies a set of telegrapher's equations with a characteristic impedance Z_{0ppl}, which varies with the radial distance [13]. The corresponding modal voltage and current waves can be written as

$$V(\rho) = V^+ H_0^{(2)}(k\rho) + V^- H_0^{(1)}(k\rho) \tag{2a}$$

$$jZ_{0ppl} I(\rho) = V^+ H_1^{(2)}(k\rho) + V^- H_1^{(1)}(k\rho) \tag{2b}$$

$$Z_{0ppl} = \frac{\eta h}{2\pi\rho} \tag{2c}$$

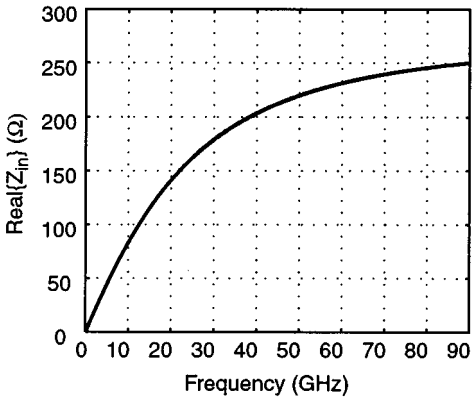
where $\eta = \sqrt{\mu/\varepsilon}$ is the intrinsic impedance of the medium. From these equations, the general relation for the input impedance of a radial transmission line can be derived. Similar to a regular transmission line, network parameters, such as the admittance Y-parameters, for a section of a radial transmission line can be calculated. To solve this problem, modifications have been introduced in the derivation of the Y network parameters originally reported by Marcuvitz [13] to exclusively involve Hankel functions. The motivation for this choice is that Hankel functions exhibit numerically stable behavior as opposed to Bessel functions, which lead to expressions with zeros (poles). The detailed expressions for the used Y-parameters of a radial transmission line are shown in Appendix A.

An interesting feature of radial transmission lines is that the characteristic impedance for the infinite line is not the same as its input impedance [13]. Indeed, the normalized input admittance looking at the radial distance ρ is

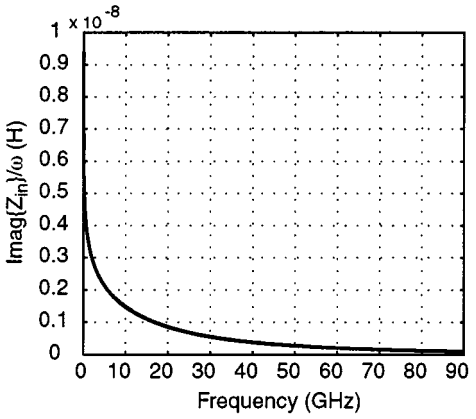
$$Y(\rho) = -j\frac{H_1^{(2)}(k\rho)}{H_0^{(2)}(k\rho)} \tag{3}$$

which is normalized to the characteristic impedance at the location ρ defined in (2c). Fig. 1 shows the variation of the input impedance $Z_{in} = Z_{0ppl}/Y(\rho)$ of an infinite radial transmission line seen at $\rho = 0.5$ mm away from the center. It can be concluded from Fig. 1 that, as the frequency increases, so does the magnitude of the input impedance. On the other hand, the noise voltage at the input port of an infinite radial transmission line is obtained by multiplying this impedance with the input current to the parallel plates. Therefore, the noise voltage becomes higher with increasing frequency.

Fig. 1 is also interesting to the problem at hand in two other respects. First, at lower frequencies, the input impedance becomes predominantly reactive, which resembles the case of a transmission line at cutoff. Nevertheless, the "cutoff" frequency of the dominant mode is 0 Hz and, therefore, the dc component is conducted as it should. Second, as Fig. 1 shows, the impedance of the radial transmission line exhibits a reactive component. It can be argued that this reactive component is responsible for describing well the near fields of a via. Indeed, the wave admittances of the higher order cylindrical modes, at the quasi-static limit $k \to 0$, correspond to negligibly small values and, thus, the reactive near field is dominated by the fundamental TM_{00} mode [15]. This is in contrast to the case of treating the input impedance of a probe in a rectangular waveguide, which requires including a great number of evanescent modes in order to predict its imaginary part. This point-of-view is supported by the high accuracy of the proposed single-mode CAD models, as will be verified in the subsequent sections of this paper.



(a)



(b)

Fig. 1. Input impedance of an infinite-length radial transmission line. The radius of the observation point is 0.5 mm, $h = 4.62$ mm, and $\varepsilon_r = 4.15$. (a) Real part and (b) imaginary part normalized to $\omega = 2\pi f$.

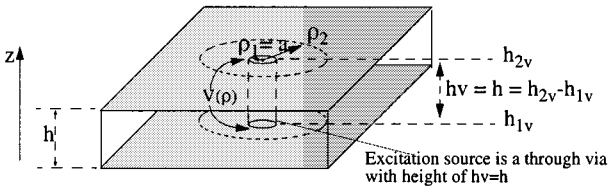


Fig. 2. Parallel-plate waveguide with a via.

B. Coupling From a Via to the Parallel Plates

In the formulation of the previous section, $V(\rho)$ is the voltage between the parallel plates, which is equal to the voltage of the excitation source (across the via) shown in Fig. 2 when ρ is equal to the radius of the via. In the derivations of Section II-A, the excitation current (via current) is assumed to be vertically directed (along z) with no dependence on the spatial variables ρ, ϕ, and z. However, when the height of the via (hv) is less than the spacing between the parallel plates (h), as in a buried via configuration, a variation along the z-axis is introduced for the excitation current.

For a through via, the excitation current of the parallel-plate waveguide is equal to the via current, while for a buried configuration, the via current is only partially coupled to the plate current. Consider the buried via interconnecting two striplines in an infinite parallel-plate environment shown in Fig. 3. A charge imbalance on the parallel plates occurs during the signal passage

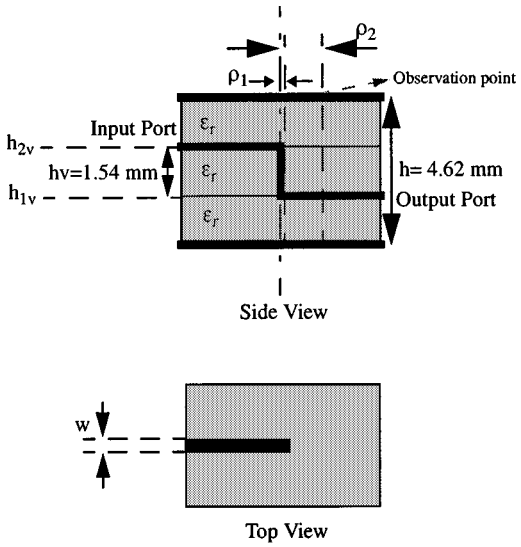


Fig. 3. Studied buried via structure [3].

through the via and results in voltage fluctuations on the plates. From another perspective, this happens when the stripline mode hits the via and part of its energy transfers to cylindrical waves supported by the parallel plates. To model this partial coupling, a β factor can be introduced, which can be derived from a static field capacitance calculation [3], [10].

The derivation of the coupling factor β for the radial transmission-line mode directly from field relations is shown in Appendix B. The final result when the via current is defined by $I(z) = I_0 j(z)$ in (B1) is as follows:

$$\beta = \frac{1/h \int_{h_{1v}}^{h_{2v}} I(z)\, d(z)}{I_0}. \tag{4}$$

Note that, for a constant via current, the coupling factor β only depends on the geometry of the problem at hand in a trivial way. For example, in the case of the geometry shown in Fig. 3, $\beta = hv/h = 1/3$.

III. MODELING

A. Single Via Structures

To explain the proposed models, first consider the simple case of the stripline-via structure shown in Fig. 3. The corresponding proposed model is shown in Fig. 4(a). The intrinsic via is modeled by the well-known Π circuit, interconnecting two striplines of characteristic impedance Z_0. The values for the inductance and capacitance of the via [L_x and C_x in Fig. 4(a)] were extracted through optimum matching of the scattering parameters obtained from a moment-method-based full-wave analysis of the structure in Fig. 3, with those from circuit simulations in the frequency domain. The current flowing through the via is coupled to the parallel plates by means of a dependent current source. On the other hand, the reciprocal induction of the parallel-plate mode back to the signal is included by using a dependent voltage source [3], [10]. The two dependent voltage and current sources correspond to an ideal transformer with a turn-ratio equal to the coupling coefficient β defined in (4).

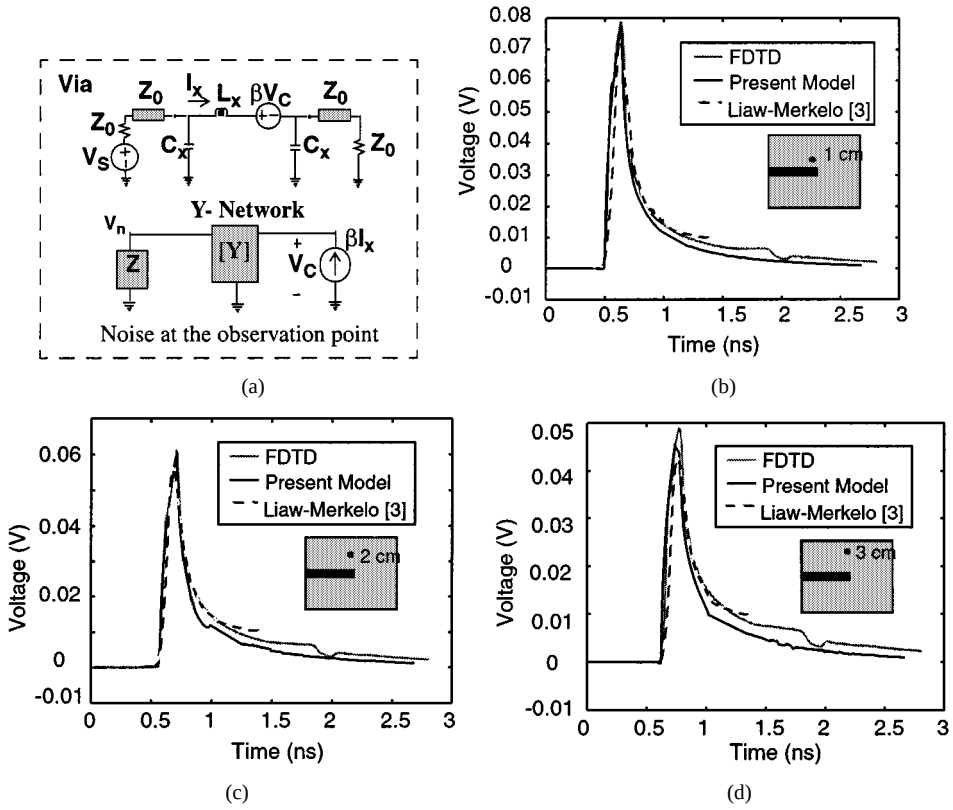


Fig. 4. (a) Proposed lumped-element via model based on radial transmission-line theory. Noise voltage at different distances from the central axis of the via at: (b) 1 cm, (c) 2 cm, and (d) 3 cm.

Applying the theory presented in Section II, the ground planes of the stripline structure are modeled as an infinite radial transmission line with an excitation source at its center to represent the presence of the via. The section of the radial transmission line connecting the input port at the radius of the via (ρ_1 in Fig. 3) to the observation point (ρ_2 in Fig. 3) is represented by a delay element designated with "Y-network" in Fig. 4(a). This delay element is a two-port network characterized by the admittance parameters of the section of the radial transmission line between ρ_1 and ρ_2 in Fig. 3. The pertinent admittance elements are obtained from (A1a)–(A1d) in Appendix A. Furthermore, the terminating impedance Z is dependent on the geometry of the substrate. For infinite (relatively large) substrates, Z is the input impedance of an infinite radial transmission line calculated at the observation point obtained from (3), i.e., $Z = Z_{0ppl}/Y(\rho)$.

1) Validation: The dimensions for a stripline-via structure were chosen as in [3], where $\mathrm{hv} = 1.54$ mm, $\mathrm{h} = 4.52$ mm, $\varepsilon_r = 4.15$, and the via is considered as a 2-mm-wide conducting strip. The final lumped-element circuit shown in Fig. 4(a), was ported in Agilent-ADS and was excited with a 1-V step voltage source (Vs), having a 10%–90% rise time equal to 115 ps. The simulation time of this circuit was on the order of a few seconds on an Ultra 5 SUN workstation, which is a substantial reduction in comparison with the hours of simulation time needed for a full-wave 3-D technique such as the FDTD on the same platform, as well as the simulation time reported in [3], corresponding to a 2-D *LC* ladder network model for the parallel plates. The noise voltage between the parallel plates has been observed at points with distances of 1, 2, and 3 cm from the center of the via [see Fig. 4(b)–(d)]. The accuracy of the model was also demonstrated by comparison with FDTD simulations with the same 1-V step excitation located at the input port shown in Fig. 3 and the results presented in [3].

2) Extension to Multiple Parallel-Plate Environments: The model has been extended to include multiple layers in a through via case. Fig. 5 shows the single via structure and the proposed lumped-element model. The through via interconnects two symmetrical striplines with one common ground plane in a dual parallel-plate environment. Therefore, the excess capacitance and inductance of the via are the same as those in each individual stripline region. However, a parasitic capacitance C_{x2} has to be included in order to model the parasitic effect of the ground aperture in the common ground plane. The values for C_{x1}, L_{x1}, and C_{x2} are derived from matching the scattering parameters of the structure in Fig. 5(a), obtained from a full-wave simulation, with the scattering parameters of the circuit for frequencies below 5 GHz. The so-determined values for the inductors and capacitors have been used to port the circuit model of Fig. 5(b) in Agilent-ADS and subsequently a transient simulation was performed. This yielded the noise voltage in the two regions of the parallel plates, as shown in Fig. 6, along with validating FDTD simulations. Note that the noise peak for the bottom parallel plates is slightly smaller than what was obtained for the top plate at the same distance from the via. The reason for this is the relatively smaller current flowing in the part of the via buried in the bottom layer due to the current drawn by C_{x2} representing the fringing fields of the aperture.

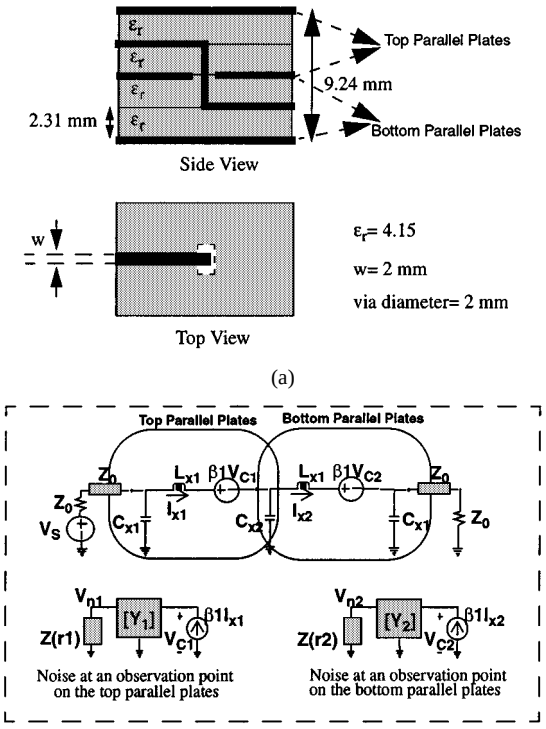


Fig. 5. (a) Multilayer through stripline-via structure. The size of the aperture on the common ground plane is 6 mm × 6 mm. (b) Proposed lumped-element model based on radial transmission-line theory.

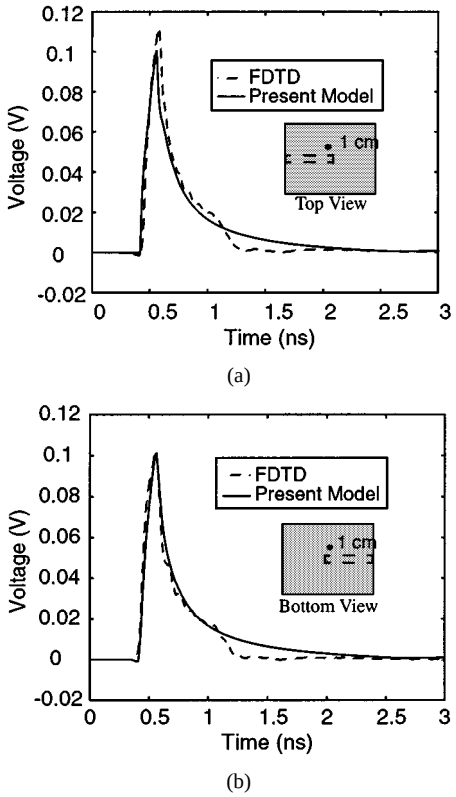


Fig. 6. Noise voltage between the parallel plates observed at 1 cm away from the central axis of the via. (a) Top planes. (b) Bottom planes.

B. Multiple Via Structures

The model has also been extended to include crosstalk between multiple vias and reflections from substrate edges.

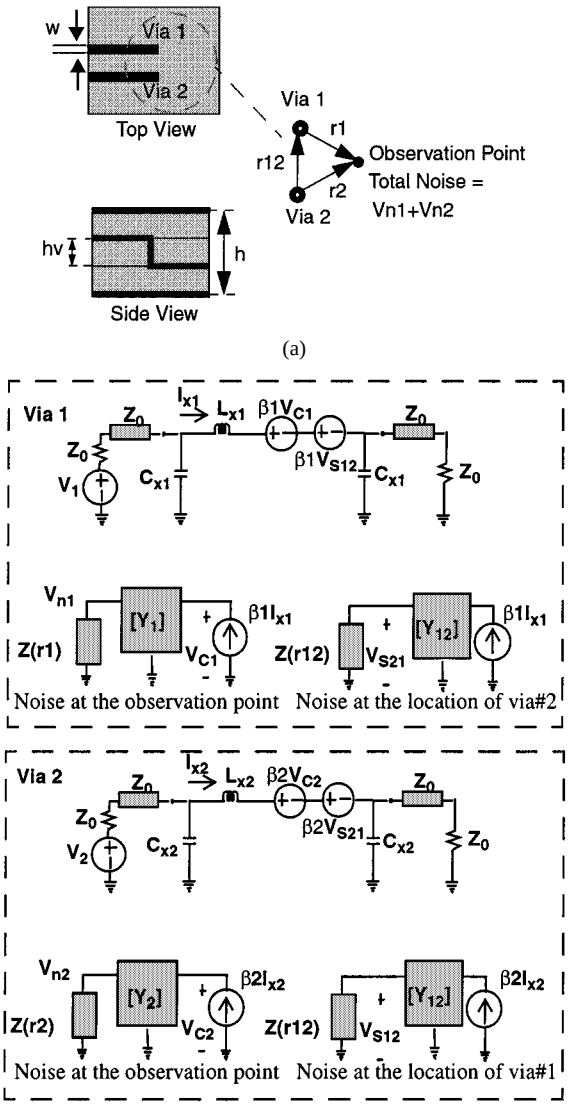


Fig. 7. (a) Multiple stripline-via structure. (b) Equivalent circuit for multiple stripline-via structure.

Fig. 7 shows a two stripline-via structure and the proposed lumped-element model. This circuit consists of two single stripline-via structures, which are coupled only through the excited TEM parallel-plate mode. The Y-network elements (Y_{12}, Y_{21}, Y_1, and Y_2) and the location-dependent terminating impedances [Z(r1), Z(r2), and Z(r12)] shown in Fig. 7(b), represent different points on the parallel plates and are obtained using relations (A1a)–(A1d) (see Appendix A), and (3). The total noise voltage is the superposition of V_{n1} and V_{n2}, the corresponding noise voltages at the observation point due to each via. The excited parallel-plate wave by each via is intercepted by the other via inducing a voltage on the victim line [6], [7], [11]. This coupling mechanism is included in the prototype model by the dependent voltage sources $\beta 1 V_{S12}$ and $\beta 2 V_{S21}$. The dimensions of the substrate, vias, and striplines are the same as those of the single via structure of Fig. 3. Firstly, in order to monitor the effect of increasing the frequency content of the input signal on the noise level, the rise time of the input step source for the single stripline-via structure of Fig. 3

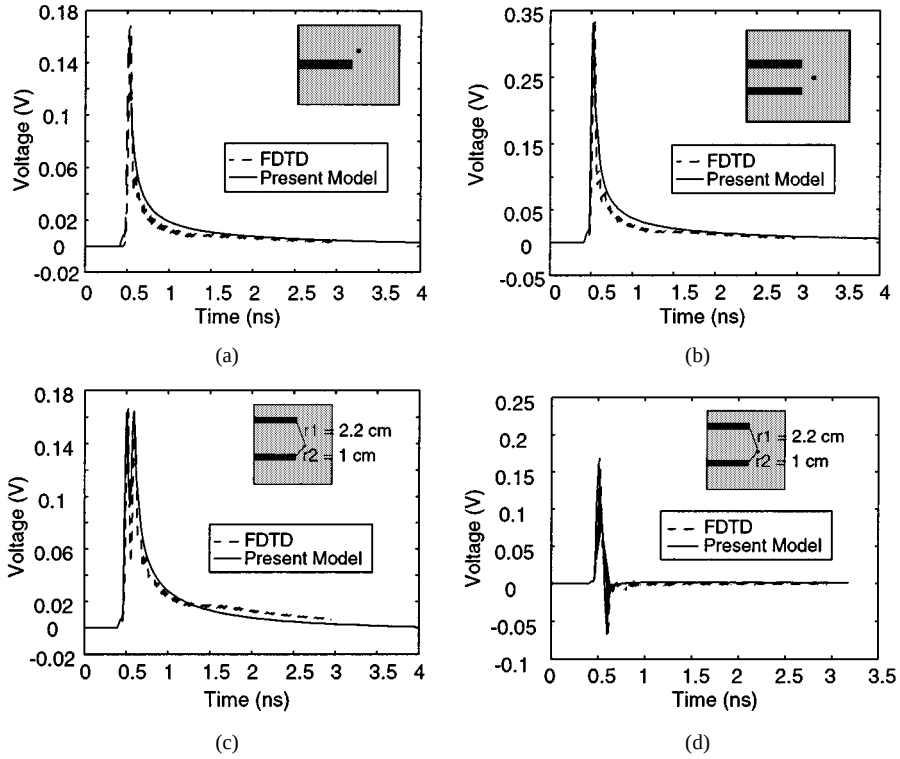


Fig. 8. Noise voltage for different structures, but all with a 40 ps (0%–100%) rise time for the excitation step pulse sources. (a) Single stripline-via structure at 1 cm away from the via. Two-stripline-via structure: (b) common-mode excitation $\mathrm{r1} = \mathrm{r2} = 1$ cm, (c) common-mode excitation $\mathrm{r1} = 2.2$ cm and $\mathrm{r2} = 1$ cm, and (d) differential mode excitation $\mathrm{r1} = 2.2$ cm and $\mathrm{r2} = 1$ cm.

has been reduced to 40 ps (0%–100%). In the corresponding simulation result shown in Fig. 8(a), it can be seen that the noise peak is almost twice the noise peak obtained for a 115 ps (10%–90%) rise time, as shown in Fig. 4(b). Keeping this faster rise time for the voltage sources in the equivalent circuit of the two stripline-via structure, common-mode (even) and differential-mode (odd) excitations have been investigated. For the case of common-mode excitation and for an observation point at the same distance from the two vias (the spacing between the vias is 1.4 cm), the noise peak is doubled as compared to a single via, as shown in Fig. 8(b). For this case, the generated noise peaks from each via have the same amplitude and delay. To distinguish the two noise peaks, the two distances $\mathrm{r1}$ and $\mathrm{r2}$ (shown in Fig. 7) from the observation point were chosen to be different at 2.2 and 1 cm, respectively. The spacing between the vias is 2.8 cm in this configuration. The simulated noise voltages for common and differential mode excitations are shown in Fig. 8(c) and (d), respectively. As can be observed in Fig. 8(c), the two noise peaks do indeed separate. On the other hand, for the odd-mode excitation, the generated noise voltages cancel each other at certain directions, resulting in voltage nulls on the plates. This concept can be applied in the pin assignment of multichip modules and for isolating sensitive devices from noise in particular cases. All circuit simulations have been performed using Agilent-ADS and verified with FDTD simulations, as shown in Fig. 8. Further investigation of differential vias has been performed by extending the model presented in Fig. 7(b) to differential through vias in multilayer parallel-plate environments [16]. In [16], it has been demonstrated that further reduction of the noise peak is achievable by choosing a closer spacing between the differential vias.

C. Measurement Results

In order to fully validate the developed models, representative test boards have been constructed and tested using a TDR setup. The TDR system comprises an HP 54124A digitizing oscilloscope and an HP 54120B test set. The system utilizes a square-wave generator with a 50-kHz repetition rate. The duty cycle of the square wave is 50% and, thus, the pulse duration is long enough to be considered as a step voltage. The rise and fall times are about 40 ps (10%–90%) measured at the input channel of the test set.

1) Infinite Planes: First, the proposed multiple structure model was verified through measurements based on the assumption of infinite planes. For this purpose, a relatively large FR4 board (33 cm $\times$ 33 cm) containing a single stripline-via structure was fabricated. A probe placed 1 cm away from the center of the via was used to measure the voltage between the parallel plates, as shown in Fig. 9(a). The substrate parameters of the test board were $\mathrm{hv} = 1.54$ mm, $\mathrm{h} = 4.52$ mm, and $\varepsilon_r = 4$, while the linewidths were 2 mm, and the via diameter was 1 mm. The probe for detecting the voltage between the parallel plates can be considered as a second (passive) through via terminated to 50 Ω. Therefore, the probe is represented using the multiple structure model of Fig. 7, by setting the coupling factor $\beta 2$ to one, taking out the independent voltage source and the transmission-line sections and shorting out the Z_0 termination, as shown in Fig. 9(b). The simulation and measurement results are shown in Fig. 9(c), where the input signal

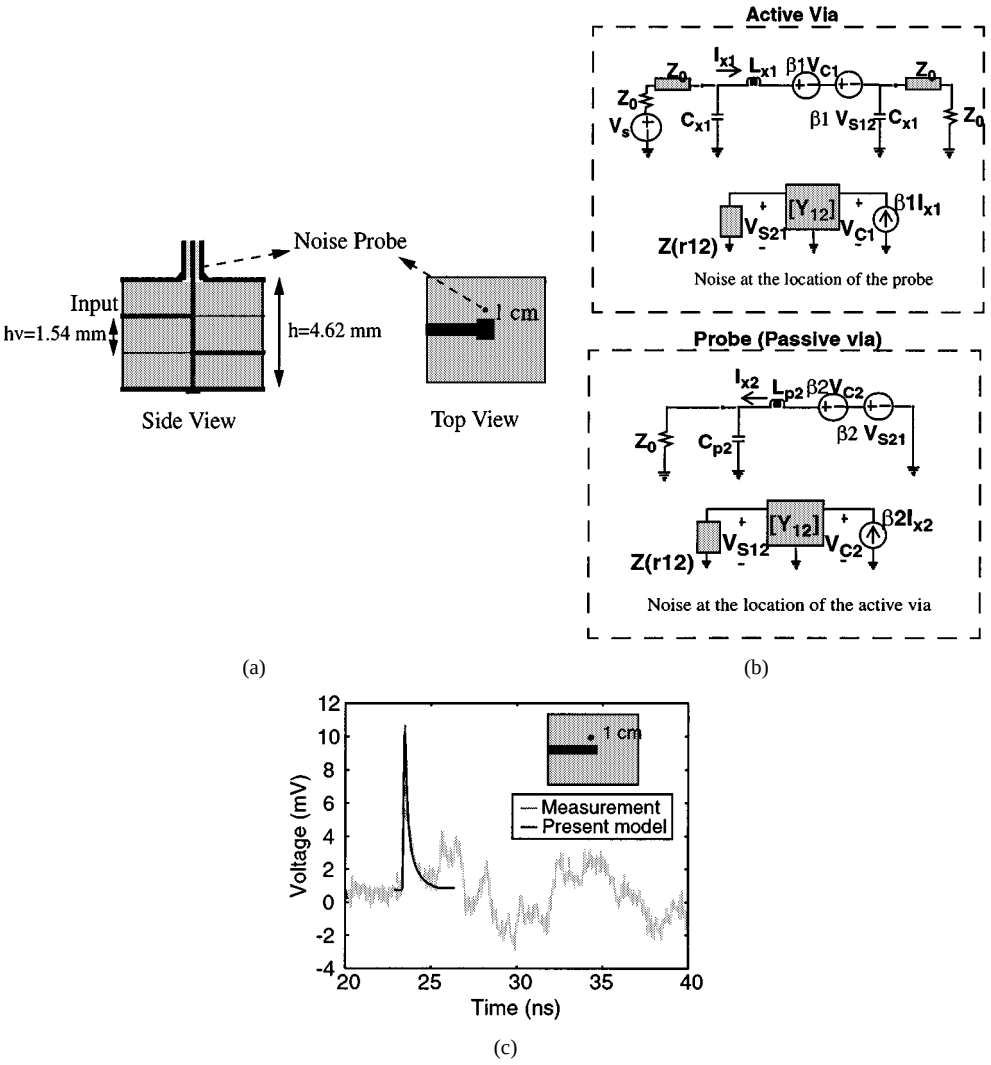


Fig. 9. (a) Stripline-via structure under test. The diameter of the via is 1 mm and the via pad is a 4 mm × 4 mm square. The striplines are 2-mm wide, and $\varepsilon_r = 4$. (b) The developed model for the tested buried via structure. (c) Measured and simulated parallel-plate noise.

is a 0.4-V step voltage source V_1 with 40-ps 10%–90% rise time. The result shows an excellent accuracy in the prediction of the first peak, which is the most prominent characteristic of the noise signature. The rest of the measured noise waveform is shaped by reflections from the edges of the board, a situation which is treated in the following section.

2) Finite Substrates: A second test board was fabricated to investigate the parallel-plate mode excitation for through vias in finite substrates, as shown in Fig. 10(a). The board was a 10 cm × 10 cm double-sided FR4 covered with solid conductor plates. The active through via was located at the center of the board and the observing through via at 3 cm away from the center. The height of the board was 1.56 mm, $\varepsilon_r = 4$, and the diameters of the vias were 1.3 mm. The edges are considered as perfect magnetic walls reflecting the voltage waves with the same phase [4], [6], [7], [17]. The launched signal is a 0.4-V step voltage source with 40-ps 10%–90% rise time. The reflections from the substrate edges are included by assuming an infinite parallel-plate environment and introducing images of the active via, thus reducing the situation to the multiple via model of Fig. 7 (with $\beta = 1$). The diagram of the employed images is shown in Fig. 10(b). The transmitted signal to the passive via is shown in Fig. 10(c) when only eight images are used, corresponding to reflections reaching the probe within 1.1 ns after the beginning of the transient simulation. If it is desired to predict the noise for a longer duration, more images should be included. The simulation time for this structure requires less than 1 min on an Ultra 5 SUN workstation.

3) Including Decoupling Capacitors: For the connection of a decoupling capacitor, another through via was added to the smaller test board (10 cm × 10 cm), 1 cm away from its center, as shown in Fig. 11(a). To maximize the noise cancellation, decoupling capacitors are usually placed as close as possible to the source of the noise. In this way, the parallel-plate fields generated by the via of the decoupling capacitor are out of phase with those from the active via and tend to cancel out. For modeling this situation, another passive via terminated by a capacitor is added to the multiple via configuration of Fig. 7. The corresponding images of this new through via are also included to correctly capture the noise signature in the time span of interest, which is 1.1 ns after the beginning of the transient simulation. From the simulations, it was found that for values larger than 1 pF, the noise voltage at the 3-cm observation point starts diminishing, and by increasing the capacitance to about 100 pF,

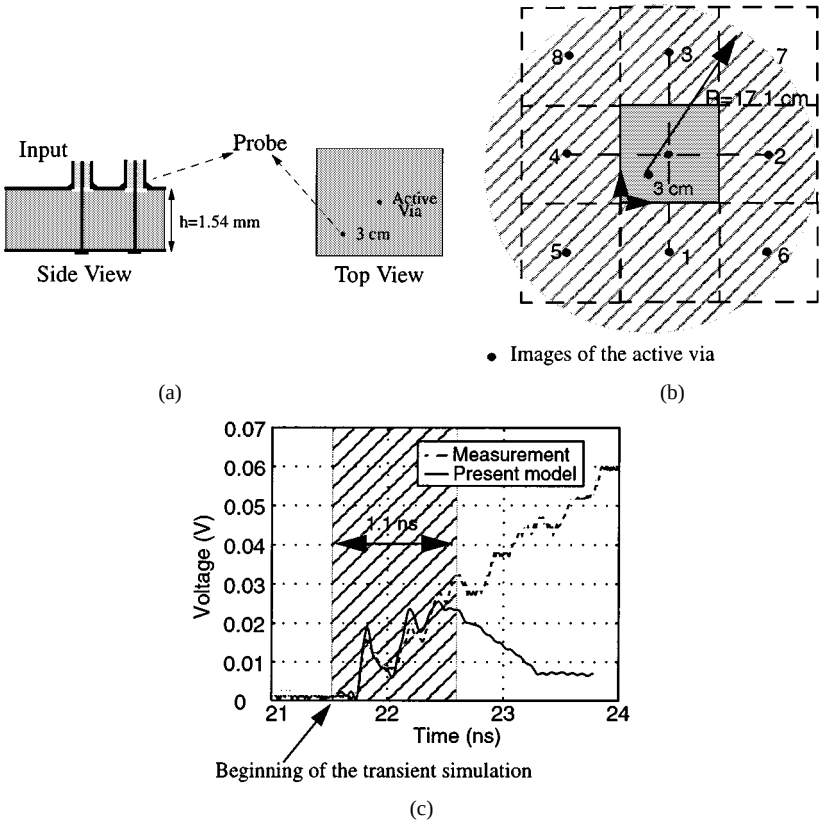


Fig. 10. (a) Through via structure under test. (b) Diagram of the employed images. (c) Measured and simulated parallel-plate noise. The observation via is 3 cm away from the board center.

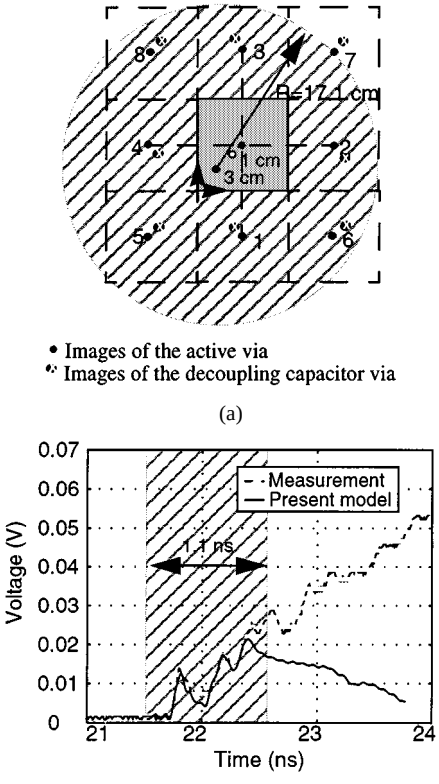


Fig. 11. (a) Diagram of the employed images. (b) Measured and simulated parallel-plate noise with a 100-pF decoupling capacitor located 1 cm away from the board center.

it reaches the minimum peak level. Higher capacitances did not improve the noise suppression. Therefore, a 100-pF surface mount decoupling capacitor was used in the measurements. The measured and simulated noise waveforms results are shown in Fig. 11(b). Further TDR experiments on this board with different capacitor values (1, 100, and 200 nF) also agreed with the simulation predictions, but are not shown here for brevity.

In order to further minimize the noise level at the observation point, another decoupling capacitor was added to the circuit. Since the first capacitor was already placed as close as possible to the source (the active via), the distances r1 and r2 in Fig. 12(a) are known. On the other hand, the location of the second capacitor is defined by its distances from the source and the observation point, i.e., ρ_1 and ρ_2 in Fig. 12(a), respectively, which are the unknowns. The location and value of this capacitor should be chosen in a way that enhances the effect of the first capacitor. For this purpose, the delay and amplitude of the parallel-plate noise generated by the via connected to the second capacitor should be the same as those of the parallel-plate noise generated by the via connected to the first capacitor. Therefore, the constraints imposed by the first decoupling capacitor on the delay and amplitude of the parallel-plate mode excited by the second capacitor determine ρ_1 and ρ_2, as expressed by the following relations:

$$\rho_1.\rho_2 = r1.r2 \tag{5a}$$

$$\rho_1 + \rho_2 = r1 + r2 \tag{5b}$$

For the structure shown in Fig. 12(a), where $\mathrm{r1} = 1$ cm and $\mathrm{r2} = 2$ cm, the distances ρ_1 and ρ_2 can be derived from (5) as

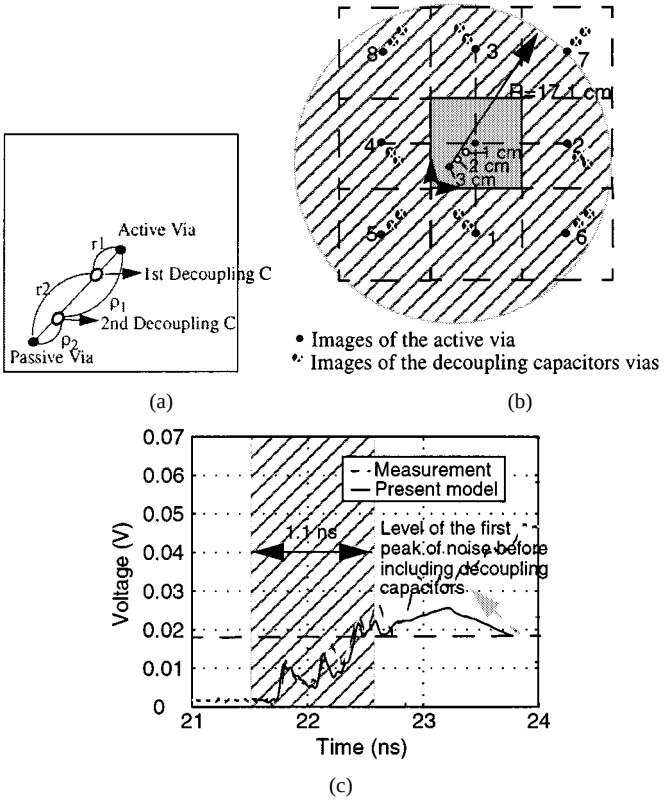


Fig. 12. (a) Diagram showing the location of the decoupling capacitors and the active via. (b) Diagram of the employed images. (c) Measured and simulated parallel-plate noise with two 100-pF decoupling capacitors located 1 and 2 cm away from the board center.

2 and 1 cm, respectively. To model the effect of the decoupling capacitors, the images of both of the vias used for the connection of the capacitors should also be included in the image diagram, as shown in Fig. 12(b). Focusing on the reflections reaching the observation probe within about 1.1 ns after the beginning of the transient simulation results in a total number of 22 images. The simulation was performed by implementing the multiple via model in Agilent-ADS and including all 22 images. The corresponding simulation time on an Ultra 5 SUN workstation was less than 2 min. It should be pointed out that the value of the second capacitor was chosen based on successive simulations for obtaining the minimum noise peak and the closest available value, i.e., 100 pF, was used for implementing the structure. The simulation and measurement results are shown in Fig. 12(c), exhibiting a very good agreement. The improvement in terms of suppression of the peak noise compared to the single decoupling capacitor case is small, but noticeable. To completely eliminate the noise at this observation point, more decoupling capacitors should be used and arranged in a fence-like structure or surround the source in the form of a coaxial via [18]. However, with the present approach, it is possible to bring down the noise below a threshold level for a sensitive integrated circuit (IC) with a minimum number of capacitors.

IV. Conclusions

A series of physics-based CAD models for vias in parallel-plate environments have been developed by modifying the standard Π equivalent circuit for a via to account for the coupling to the dominant TEM (TM_{00}) mode. The underlying method employed for this purpose is to model the parallel plates using radial transmission-line theory. The corresponding rigorous derivations for setting up the models have been presented. The versatility of the derived models has been verified in a number of situations, such as single and multiple buried or through vias in a multilayer environment, edge reflections from finite boards, as well as the optimization of decoupling capacitor configurations for noise suppression. In all cases, the models have been verified against data available in the literature, independent FDTD simulations, as well as TDR measurements on specific test boards. The presented models are portable to commercial circuit simulators, such as Agilent-ADS, and lead to a drastic reduction of the simulation time compared to full-wave methods such as the FDTD, while maintaining comparable accuracy. It should be pointed out that, although in this paper the lumped-element L and C values for some via configurations have been extracted using a moment-based analysis, nevertheless, standard rapid quasi-static approximations could also be utilized. The developed models are versatile in the sense that they allow to include linear and nonlinear circuit components such as decoupling capacitors or even diodes and gates. This feature enables the global simulation of entire high-speed circuits including their interconnects, as well as the prediction of the noise pattern on the parallel plates.

Appendix A

The employed Y network parameters for the radial transmission line of Fig. 2 between two points at locations ρ_1 and ρ_2 are

$$Y_{11}=\frac{1}{jZ_1}\cdot\frac{H_1^{(2)}(k\rho_1)H_0^{(1)}(k\rho_2)-H_0^{(2)}(k\rho_2)H_1^{(1)}(k\rho_1)}{H_0^{(2)}(k\rho_1)H_0^{(1)}(k\rho_2)-H_0^{(2)}(k\rho_2)H_0^{(1)}(k\rho_1)} \tag{A1a}$$

$$Y_{12}=\frac{1}{jZ_1}\cdot\frac{H_0^{(2)}(k\rho_1)H_1^{(1)}(k\rho_1)-H_1^{(2)}(k\rho_1)H_0^{(1)}(k\rho_1)}{H_0^{(2)}(k\rho_1)H_0^{(1)}(k\rho_2)-H_0^{(2)}(k\rho_2)H_0^{(1)}(k\rho_1)} \tag{A1b}$$

$$Y_{21}=\frac{1}{jZ_2}\cdot\frac{H_0^{(2)}(k\rho_2)H_1^{(1)}(k\rho_2)-H_1^{(2)}(k\rho_2)H_0^{(1)}(k\rho_2)}{H_0^{(2)}(k\rho_1)H_0^{(1)}(k\rho_2)-H_0^{(2)}(k\rho_2)H_0^{(1)}(k\rho_1)} \tag{A1c}$$

$$Y_{22}=\frac{1}{jZ_2}\cdot\frac{H_1^{(2)}(k\rho_2)H_0^{(1)}(k\rho_1)-H_0^{(2)}(k\rho_1)H_1^{(1)}(k\rho_2)}{H_0^{(2)}(k\rho_1)H_0^{(1)}(k\rho_2)-H_0^{(2)}(k\rho_2)H_0^{(1)}(k\rho_1)} \tag{A1d}$$

where $Z_1=\eta h/2\pi\rho_1$, $Z_2=\eta h/2\pi\rho_2$, and $k=\omega\sqrt{\mu\varepsilon}$. It should be mentioned that, for a multilayer substrate with layers of different dielectric constants sandwiched between two plates, quasi-static formulas for the Z_1, Z_2, and Y-parameters can be obtained by treating the per-unit-length capacitance for each layer as a series cascade arrangement. The formulation based on this approach has been developed in [19] and utilized for modeling multilayer ball grid arrays in [6].

APPENDIX B

The coupling factor β can be determined from a rigorous field treatment. The TM_{mn} and TE_{mn} modes of a parallel-plate radial waveguide are derived in [14] and [15]. Consider a via having a radius $\rho_1 = \mathrm{a}$ with an excitation current defined by

$$I(z) = \begin{cases} I_0 j(z), & \text{if } (h_{1v} < h < h_{2v}) \\ 0, & \text{otherwise.} \end{cases} \tag{B1}$$

Since there is azimuthal symmetry, the excited TM modes are of the form TM_{0n}. The corresponding magnetic field is, therefore, given by

$$H_\phi^{(0n)}(\rho, z) = B_{0n} \frac{k}{\mu} H_1^{(2)}(k\rho) \cos\Big(\frac{n\pi}{h} z\Big) \tag{B2}$$

where $k = \sqrt{k_0^2 - (n\pi/h)^2}$ and $k_0 = \omega\sqrt{\mu\varepsilon}$. In order to find the B_{0n} coefficients, Ampere's law can be applied on the surface of the via, yielding

$$\int_0^{2\pi} \sum_{n=0}^{\infty} H_\phi^{0n}(a, z) a d\phi = I(z). \tag{B3}$$

Using the orthogonality of the $\cos(n\pi z/h)$ functions in (B3) results in

$$B_{0n} = \frac{\mu}{\epsilon_n k h \pi a H_1^{(2)}(ka)} \int_{h_{1v}}^{h_{2v}} I(z) \cos\Big(\frac{n\pi}{h} z\Big) dz \tag{B4}$$

where $\epsilon_0 = 2$ and $\epsilon_n = 0$ if $n \neq 0$. With reference to Fig. 4(a), the corresponding coupling factor can be described in a natural way as the ratio of the dominant-mode ($\mathrm{n} = 0$) parallel-plate current to the via current. This represents the "turn ratio" of the ideal transformer modeled with the dependent voltage and current sources in Fig. 4(a). Therefore, β is given by

$$\beta = \frac{H_\phi^{0n}(a) 2\pi a}{I_0}. \tag{B5}$$

From (B2), (B4), and (B5), this yields

$$\beta = \frac{\dfrac{1}{h} \displaystyle\int_{h_{1v}}^{h_{2v}} I(z)\, dz}{I_0}. \tag{B6}$$

Note that if $I(z) = I_0$, i.e., a constant, then β is simply given by

$$\beta = \frac{h_{1v} - h_{2v}}{h}. \tag{B7}$$

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