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Equivalent circuit for multiple vias in parallel plate environment

R. Abhari, G.V. Eleftheriades and T.E. van Deventer

An equivalent one-dimensional circuit has been developed to model the loading effects of vias (through or buried) in a parallel plate environment. Owing to the one-dimensional nature of the model, the simulation time is dramatically reduced, compared to either two-dimensional inductance-capacitance ladder network or full-wave numerical electromagnetic simulations. This model can be easily included in available commercial circuit simulators and accounts for multiple via interactions as well as for substrate edge reflections.

Introduction: Traditionally, a via discontinuity has been modelled with a Π-network consisting of a series inductance and two excess capacitances to the ground to predict the reflection on the signal path [1]. When a via goes through or is buried between two reference voltage (power/ground) planes, the parallel plate transverse electromagnetic mode (TEM) mode is excited. This TEM mode manifests itself as a voltage fluctuation on the two reference voltage planes and is generally referred to as noise. Much of the research work has focused on modelling and analysing the parallel plate environment [2 – 5]. In one approach, a two-dimensional inductance-capacitance (LC) ladder network was used to model the parallel plates, leading to excessive computational times are associated with fully numerical techniques, such as the finite difference time domain (FDTD) analysis [2]. Hybrid methods which combine full-wave numerical techniques with lumped-element ladder models can also lead to excessive computational times for large and complex circuits and require the development of dedicated CAD tools [3, 4]. An efficient way of representing the effect of the parallel plates is to apply radial transmission line (RTL) theory [5]. However, work that has been reported so far is based on RTL theory and is in analytical form, and therefore is not suitable for integration with popular circuit simulators.

In this Letter, a one-dimensional lumped-element model for vias in a parallel plate environment has been developed, based on RTL theory. The model can be easily integrated with available commercial circuit CAD tools capable of performing transient/convolution simulations. This versatile model covers both partial coupling to the parallel plate mode for a stripline via structure and parallel plate mode excitation for a through via. The proposed one-dimensional lumped-element model fully accounts for the interaction between the generated parallel plate noise and the signal power as well as the coupling between vias, while resulting in a drastic reduction of the computational time compared to either full-wave numerical analysis techniques or two-dimensional circuit models. The model has been implemented based on the popular HP-ADS circuit simulator and was extended to include substrate edge reflections, eliminating the need to utilise dedicated and time consuming full-wave numerical techniques, while maintaining a comparable accuracy.

Analysis and modelling: Fig. 1 shows a two stripline via structure and the proposed lumped element model for this configuration. The multiple via case is a minor extension of the situation presented in Fig. 1. The model consists of single stripline via structures which are coupled through the excited TEM parallel plate mode. The representative circuit for a single structure is the conventional Π equivalent circuit for a via, modified to include the loading of the parallel plates [6]. The partial coupling of the via current to the parallel plate mode is shown by the coefficient β, which can be computed from static field calculations [2]. The reciprocal induction of the parallel plate mode back to the signal is included by using the indicated dependent voltage sources $\beta 1 V_{C1}$ and $\beta 2 V_{C2}$. The Y network elements ($Y12$, $Y21$, $Y1$, and $Y2$) and the location dependent terminating impedances ($Z(r1)$, $Z(r2)$, and $Z(r12)$) shown in Fig. 1*b*, represent different points on the parallel plates and are derived by applying radial transmission line theory [7]. Furthermore, Z_o is the characteristic impedance of the stripline system, assumed to be 50Ω. The corresponding noise at the observation point from each via is referred to as V_{n1} and V_{n2}. On the other hand, each of the excited parallel plate cylindrical waves is intercepted by the other via and couples to the corresponding signal line. This latter coupling mechanism is included in the prototype model by adding another dependent voltage source in each signal line $\beta 1 V_{S12}$ and $\beta 2 V_{S21}$ as shown in Fig. 1*b*. Finally, the quantities V_{S12} and V_{S21} represent the potential difference between the parallel plates at the location of the victim via.

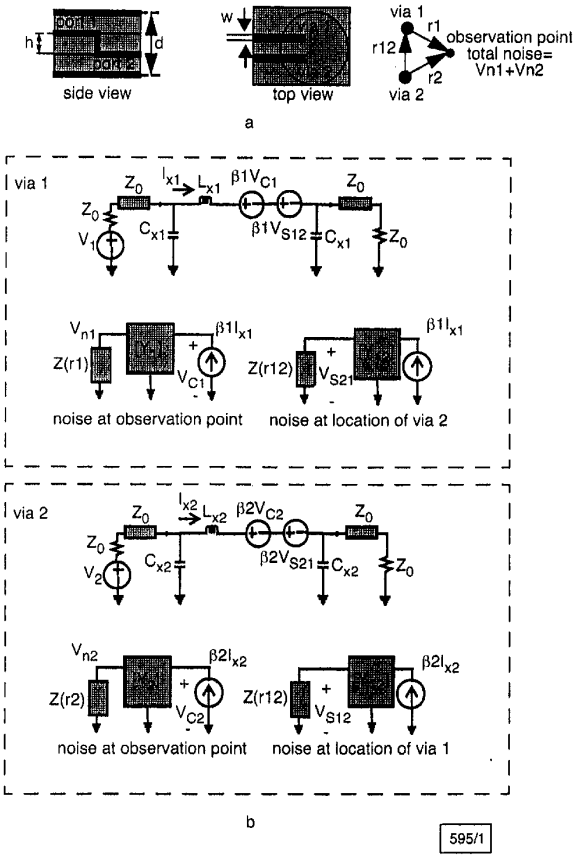

Fig. 1 *Multiple stripline-via structure and equivalent circuit for multiple stripline-via structure*

a Multiple stripline-via structure
b Equivalent circuit for multiple stripline-via structure

Simulation and measurement results: The results of time domain reflectometry (TDR) measurements on two test boards are presented in this Letter and compared with simulations. First, the proposed intrinsic network topology was verified, based on the assumption of infinite planes. For this purpose, a relatively large board (33 × 33cm) containing a single stripline-via structure was fabricated. A probe placed 1cm away from the centre of the via was used to measure the voltage between the parallel plates. The substrate parameters of the test board shown in Fig. 1*a* were h = 1.54mm, d = 4.52mm, ε_r = 4, while the line widths were 2mm and the via diameter was 1mm. The modelling of the active stripline-via and the probe is based on the equivalent circuit of Fig. 1*b*. In this model, the probe is represented as a passive via. The simulation and measurement results are shown in Fig. 2, where the input signal is a 0.4V step voltage source, V_1, with 40ps 10–90% rise time. The simulation time of this circuit is only a few seconds on an Ultra 5 SUN workstation. The result shows an excellent accuracy in the prediction of the first peak, which is the most promi-

nent characteristic of the noise signature. The rest of the measured noise waveform is shaped by the reflections from the edges of the board, which is considered below.

The second test board was fabricated to investigate the parallel plate mode excitation for through vias in the case of a finite board. The board consisted of a pair of 10 × 10cm square conductor plates with two through vias, one located at the centre of the board and the other 1cm away from its centre. The height of the board was 1.56mm, ε_r = 4, and the diameter of the vias was 1.32mm. The edges are considered as perfect magnetic walls reflecting the waves with the same phase [5]. The reflections from the substrate edges are included by assuming an infinite parallel plate environment and introducing images of the active via, thus reducing the situation to the multiple via model of Fig. 1*b* (with β = 1). A diagram of the board with eight images corresponding to reflections reaching to the probe within 1 ns after the first peak is shown in Fig. 3. To predict the noise for a longer duration, more images should be included. Fig. 3 shows the measured and simulated results exhibiting a very good agreement. The simulation time for this structure is less than one minute on an Ultra 5 SUN workstation.

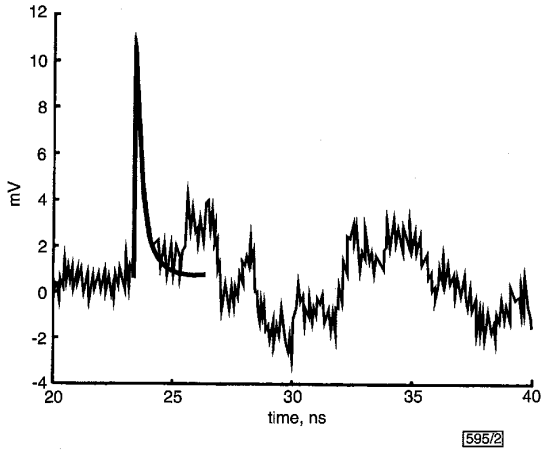

Fig. 2 *Noise voltage between parallel plates for single stripline-via structure*

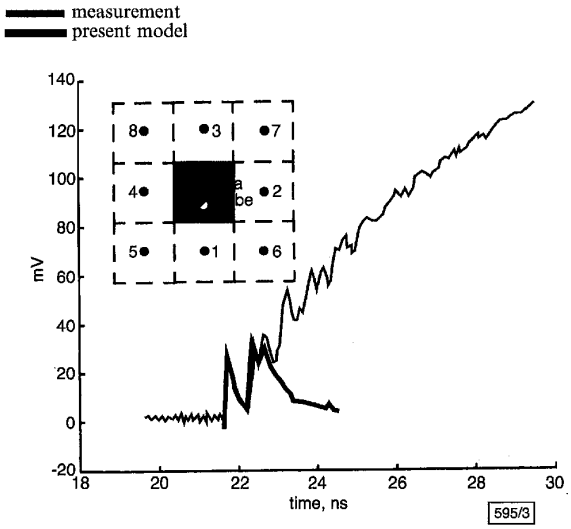

Fig. 3 *Noise voltage between parallel plates containing two through vias*

Conclusions: Based on radial transmission line theory, a one-dimensional lumped-element model has been developed to quantify the noise voltage in a parallel plate environment containing multiple vias and accounting for edge reflections. Owing to the one-dimensional nature of the model, the simulation time is dramatically reduced compared to two-dimensional LC ladder network and full-wave numerical electromagnetic simulations. The frequency-dependent elements used to represent the parallel plates can be easily incorporated in any circuit simulator capable of performing convolution simulations such as HP-ADS. The accuracy of the proposed model has been verified by contrasting with TDR measurements for different structures containing buried and through vias.

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R. Abhari, G.V. Eleftheriades and T.E. van Deventer (*Department of Electrical and Computer Engineering, University of Toronto, 10 King's College Road, Toronto, M5S 3G4, ON, Canada*)

E-mail: gelefth@waves.utoronto.ca

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Linearising pulsewidth modulator for three-phase boost inverter

J. Chen and Khai D.T. Ngo

An analogue linearising pulsewidth modulator (LPWM) for a three-phase boost inverter is presented. It employs integrators with hold and reset to compute the switching instants. The LPWM enables the output voltages of the boost inverter, which are nonlinear with respect to duty ratio control, to track the control voltages linearly. The theory is verified by experimental data.

Introduction: A three-phase boost inverter controlled by conventional PWM techniques, such as sinusoidal PWM (SPWM) and space-vector modulation (SVM), has nonlinear relationships between the output and control voltages, preventing the output from tracking the control signal [1]. Thus, its design has been based largely on small-signal linearisation around an operating point. This technique, however, does not always yield a robust design since the operating point varies.

Recently, PWM techniques that linearise (in the large-signal sense) nonlinear converters have been described in [3, 4] for DC–DC converters or single-phase inverters. Such techniques are referred to in this Letter as LPWM (linearising pulsewidth modulation). Their practical implementation for the converters in [3, 4] is simple, requiring mainly integrators with reset, since the switches are single-pole/double-throw, i.e. each switch is controlled by one duty ratio function.

The benefits of linear control have motivated the extension of LPWM to the three-phase boost inverter [2]. This converter is unique, in that it employs two single-pole/triple-throw switches, each switch controlled by two independent duty ratio functions.