An Equivalent Circuit Based on Radial Transmission Line Theory for Multiple Vias in a Parallel Plate Environment

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Abstract

In this paper, a versatile equivalent circuit for multiple vias in a parallel plate environment using radial transmission line theory is presented. The model includes crosstalk between vias, and reflections from the edges of finite substrates and provides accurate and fast means of including decoupling capacitors.

I. Introduction

In multi-layer circuit boards and 3-D packages, vias may go through the conductor planes or be buried in between them. In such configurations, the loading effect of the via discontinuity to the signal line is not only the generation of conducted noise (reflections), but also the coupling of useful signal energy to the substrate. This phenomenon happens when a time varying or a transient (switching) current goes through the via, therefore exciting the parallel plate modes. This effect is manifested by voltage fluctuations on the reference voltage planes, often referred to as (power/ ground) noise. With the increase in the frequency content of the signals in analog and digital circuits respectively along with the reduction of the supply voltages, this noise becomes one of the significant performance limiting factors. Much research has focused on modeling and analyzing the parallel plate noise excited by vias. In general, these studies can be classified in four categories: 1) Fullwave methods: Derivation of the Green's function of a resonant cavity to model the finite substrate [1] or the numerical solution of Maxwell's equations for a 3-D problem with frequency domain or time domain fullwave techniques [2], [3]; 2) Circuit-oriented methods: Modeling the parallel plates with 2-D LC ladder networks and analyzing by a transient circuit simulator [3]; 3) Analytical methods: Solution of Maxwell's equation for the dominant mode (TEM/TM_0) of the radial wave guide and derivation of the transfer and driving point impedances [4 - 6]; 4) Hybrid methods: Combining fullwave, or measurements results with circuit simulations either through a dynamic interaction between fullwave and circuit simulators[7] or by processing the data obtained from fullwave analysis or measurements to extract circuit models and subsequent simulations[8], [9].

In this work, a combination of the 2nd and 3rd approaches has been utilized. This method benefits from the accuracy and speed of an analytical approach as well as the simplicity in incorporating the device models and circuit elements of the second approach. The proposed 1-D lumped-element model fully accounts for the interaction between the generated parallel plate noise and the signal power as well as the coupling between vias, while resulting in a drastic reduction of the computational time compared to either full-wave numerical analysis techniques or two-dimensional circuit models. Equivalent circuits for structures with finite and infinite substrates containing buried vias, through vias, and decoupling capacitors have been implemented by this modeling method on the popular HP-ADS circuit simulator and compared with measurements and FDTD simulations.

II. Analysis and Modeling

In order to incorporate the coupling to the parallel plate modes for vias in a parallel plate environment in a circuit-oriented approach, the commonly used Π model of a via should be modified to reflect this phenomenon. This loss of useful energy becomes more significant as the frequency increases. For the currently available technologies in terms of substrates and interconnects dimensions, and the frequency spectrum of the signals, almost all the coupled energy goes to the dominant TEM mode. This mode propagates a cylindrical wave [10] which justifies the modeling of the parallel plates with radial transmission line theory. The network parameters for the radial transmission line have been presented in reference [11] which have been re-evaluated using Hankel functions for developing the present model.

Single Via Modeling: To explain the model, a stripline-via structure shown in Fig. 1(a) has been considered. The via is modeled by a Π circuit interconnecting two striplines with characteristic impedance Z_0 (shown in Fig. 1(b)). The current going through the via is coupled to the parallel plates by a dependent current source. The amount of coupling

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(coupling coefficient β) can be computed from static field calculations. The reciprocal induction of the parallel plate mode back to the signal is included by using a dependent voltage source [3]. The 1-D parallel plate model consists of two sections: the delay section or the "Y-Network" and the terminating impedance "Z". The Y-Network represents the admittance parameters of a section of a radial transmission line connecting the input point (radius of the via) and the observation point. The terminating impedance Z is dependent on the geometry of the substrate. For infinite (relatively large) substrates Z is the input impedance of an infinite radial transmission line calculated at the observation point.

Validation: The dimensions for a stripline-via structure were chosen as in reference [3], where h=1.54 mm,d=4.52 mm, ε_r=4.15, w=2 mm, and the via is considered as a 2 mm wide conductor sheet. The final lumped element circuit shown in Fig. 1(b), was simulated with a 1-volt step voltage source, Vs, having 115 ps 10%-90% rise time. The simulation time of this circuit was on the order of a few seconds on an Ultra 5 SUN workstation. This is a drastic reduction in the simulation time compared to the four hours reported in reference [3] for the 2-D equivalent circuit implemented on SPICE 3f2 running on an HP 720 workstation. The noise voltage between the parallel plates has been observed at a point 1 cm away from the centre of the via (see Fig. 1(c)). The accuracy of the model was also demonstrated by comparison with FDTD simulations with the same 1-volt step excitation located at Port 1 in Fig. 1(a) and the results of reference [3].

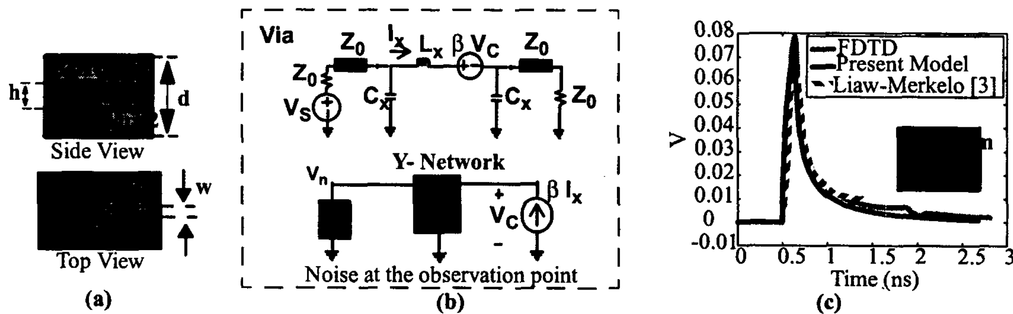

Fig. 1. (a) Stripline-via structure. (b) Proposed lumped-element model based on radial transmission line theory. (c) Noise voltage between the parallel plates observed at 1 cm away from the central axis of the via.

Extension to Multiple Vias: The model was then extended to include cross talk between vias and reflection from the edges. Fig. 2 shows a two stripline-via structure and the proposed lumped element model for this configuration. This circuit consists of two single stripline-via structures which are coupled only through the excited TEM parallel plate mode. The Y-Network elements (Y_{12}, Y_{21},Y_1, and Y_2) and the location dependent terminating impedances (Z(r1), Z(r2), and Z(r12)) shown in Fig. 2(b), represent different points on the parallel plates. The total noise voltage is the superposition of V_{n1} and V_{n2}, the corresponding noise voltages at the observation point due to each via. The excited parallel plate wave by each via is intercepted by the other via inducing a voltage on the victim line. This coupling mechanism is included in the prototype model by dependent voltage sources $\beta\ 1V_{S12}$ and $\beta 2V_{S21}$.

III. Simulation and Measurement Results

Infinite Planes: First, the proposed multiple structure model was verified based on the assumption of infinite planes. For this purpose, a relatively large board (33cmx33cm) containing a single stripline-via structure was fabricated. A probe placed at 1cm away from the centre of the via was used to measure the voltage between the parallel plates. The substrate parameters of the test board were h=1.54 mm, d=4.52 mm, ε_r=4, while the line widths were 2 mm and the via diameter was 1 mm. The probe for detecting the voltage between the parallel plates is actually a passive through via terminated to 50 Ω. Therefore, the probe is represented in the multiple structure model, by setting the coupling factor β2 to 1, taking out the independent voltage source and the transmission line sections and shorting out the Z_0 termination. The simulation and measurement results are shown in Fig. 3(a) where the input signal is a 0.4-volt step voltage source, V_1, with 40 ps 10%-90% rise time. The result shows an excellent accuracy in the prediction of the first peak which is the most prominent characteristics of the noise signature. The rest of the measured noise waveform is shaped by the reflections from the edges of the board, a situation which is treated in the following section.

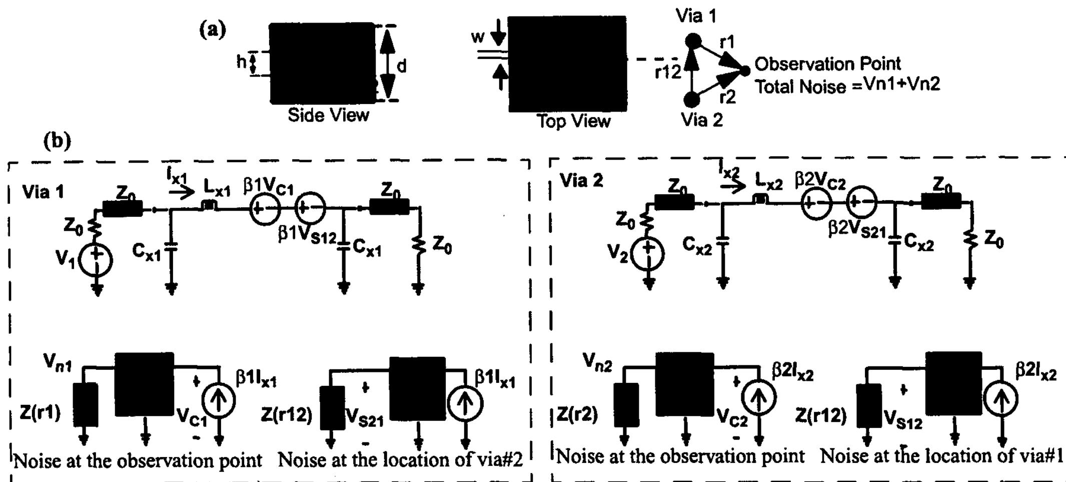

Fig. 2. (a) Multiple stripline-via structure. (b) Equivalent circuit for multiple stripline-via structure

Finite Substrate Resonances: The second test board was fabricated to investigate the parallel plate mode excitation for through vias in finite substrates. The board was a 10cmx10cm double sided FR4 covered with solid conductor plates. The active through via was located at the centre of the board and the observed through via at 3 cm away from the centre. The height of the board was 1.56 mm, ε_r =4, and the diameter of the vias was 1.32 mm. The edges are considered as perfect magnetic walls reflecting the waves with the same phase [4]. The reflections from the substrate edges are included by assuming an infinite parallel plate environment and introducing images of the active via, thus reducing the situation to the multiple via model of Fig. 2(b) (with β=1). The transmitted signal to the passive via is shown in Fig. 3(b) when 8 images corresponding to reflections reaching the probe within 1ns after the first peak have been considered in the simulations. If it is desired to predict the noise for a longer duration, more images should be included. The simulation time for this structure is less than one minute on an Ultra 5 SUN workstation. The launched signal is the same as the buried via measurement.

Decoupling Capacitors: Another through via for connection of decoupling capacitor was added to the second test board (10cmx10cm) 1cm away from the centre (shown in Fig. 3(c)). In the model this new port was included as a passive via terminated by a variable capacitor. Through transient simulations, it was found that for values larger than 1 pF the noise voltage at the 3cm observation point starts diminishing, and by increasing the capacitance to about 100 pF reaches the minimum peak noise. Higher capacitances did not improve noise suppression. Therefore, a 100 pF surface mount decoupling capacitor was used in the measurements. The measured and simulated noise waveforms results are shown in Fig. 3(d). Further TDR experiments on this board with different capacitor values (1 nF, 100 nF, 200 nF) justified the simulation predictions.

IV. Conclusions

A 1-D equivalent circuit has been developed to include the coupling to the parallel plate TEM mode in via models. This representative circuit has been extended to multiple vias thus accounting for crosstalk as well as edge reflections in finite substrates. The frequency dependent elements used to represent the parallel plates can be easily incorporated in any circuit simulator capable of performing convolution simulations such as HP-ADS. An important feature of the developed model is its versatility in including external circuit elements like decoupling capacitors or even non-linear discrete components such as diodes and gates.

Acknowledgments

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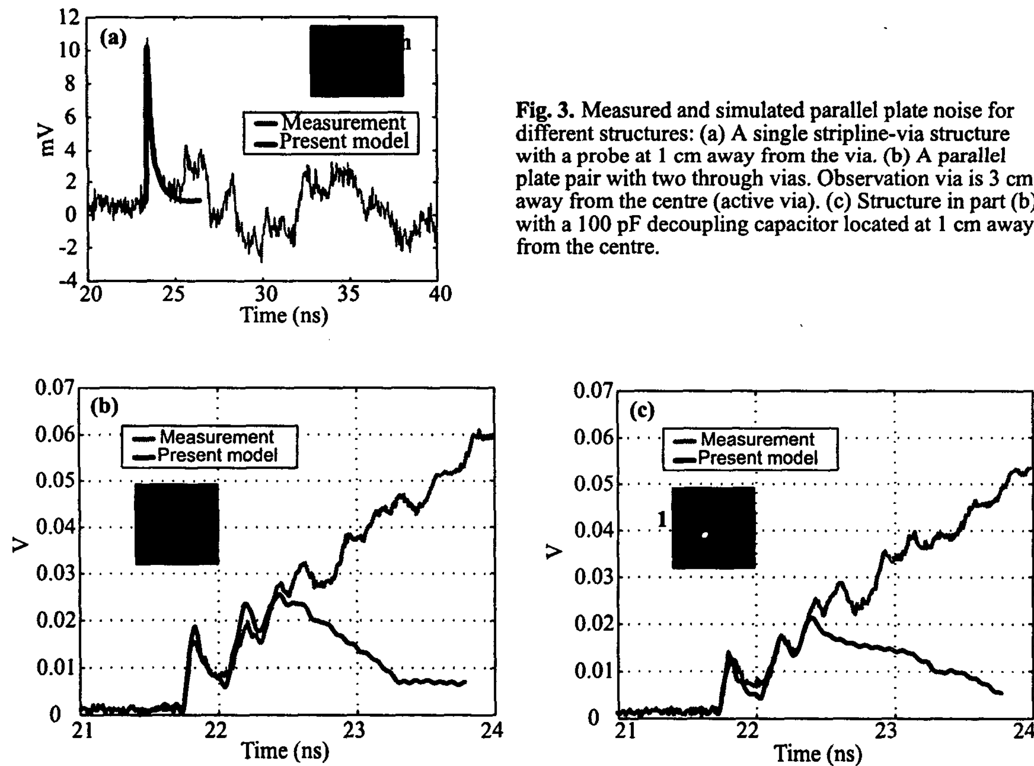

Fig. 3. Measured and simulated parallel plate noise for different structures: (a) A single stripline-via structure with a probe at 1 cm away from the via. (b) A parallel plate pair with two through vias. Observation via is 3 cm away from the centre (active via). (c) Structure in part (b) with a 100 pF decoupling capacitor located at 1 cm away from the centre.