Analysis of Differential Vias in a Multilayer Parallel Plate Environment Using a Physics-Based CAD Model

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Abstract **– A lumped-element physics-based equivalent circuit for differential vias in multilayer parallel plate environments is presented. The TEM parallel plate mode excited by differential vias is quantified by implementing the developed model in a commercial CAD tool. The corresponding CAD simulations are performed in a matter of a few seconds on an Ultra 5 SUN workstation and compare well with Time Domain Reflectometry (TDR) measurements and Finite Difference Time Domain (FDTD) simulations.**

I. INTRODUCTION

Differential interconnects are widely used in high-speed digital circuits and MMIC designs. These structures are attractive due to their inherent noise and common mode rejection features. Vias are differentially excited when interconnecting differential signal lines or when used for multiple power/ground connections supporting surge currents of opposite directions. In most of these configurations vias are buried in between or penetrating through conductor planes. The conventional Π circuit model for a single isolated via is no longer sufficient in predicting the performance of differential vias, as the coupling between the vias and the effect of the parallel plates can not be captured. Besides, these effects become even more significant in emerging high-frequency/high-speed applications. Therefore, it is necessary to develop accurate CAD models for differential vias in a parallel plate environment.

In reference [1], differentially excited vias are modeled as a cascaded network of capacitances and inductances. The capacitances are computed with a boundary integral equation technique and the inductances are calculated by employing image theory and treating the differential vias as a bifilar transmission line. This approach is recommended for geometries where the common mode current is zero and the influence of the parallel plates is negligible for inductance calculations [1]. Besides, this method does not cover the important case of differential buried vias.

In the present work, a physics-based model is proposed and verified for treating through and buried differential vias in a parallel plate environment. The model is based on the application of radial transmission line theory to represent the vias and their coupling to the parallel plate mode, and is combined with the induced EMF method to account for the mutual coupling in multiple via configurations. This approach is valid for both even and odd mode excitations. The concept of utilizing radial transmission line theory to represent vias in a parallel plate environment has been proposed before in references [2]-[4] and has been recently applied for the treatment of Ball-Grid Array packages [5]. In a more recent work by the present authors, lumped element models for multiple buried and through vias in parallel plate environments, including the coupling to the parallel plate noise and package resonances, have been developed [6]-[7].

The advantages of the proposed models in [6] and [7] can be summarized as follows; (i) they are portable to commercial circuit simulators such as Agilent-ADS, (ii) the model for the parallel plates is a 1-dimensional circuit which drastically reduces the simulation time, (iii) the simulations are accurate as the models are physics-based, (iv) the interactive coupling between the signal lines and the parallel plates is included in the model, which allows for the global simulation of the entire circuit as well as the prediction of the noise pattern on the parallel plates, (v) different types of vias such as buried, blind, and through ones can be treated.

In this paper, the models presented in [6]-[7] have been extended for the analysis of differential vias in a multilayer parallel plate environment. Validation of our approach is achieved through a set of experimental TDR measurements as well as FDTD simulations. Furthermore, the models are utilized for examining the performance of differential vias in terms of suppressing the parallel-plate noise.

II. MODELING MULTILAYER DIFFERENTIAL VIA CONFIGURATIONS

In order to study differential vias, the structure shown in Fig. 1 is investigated. This topology is chosen because it

demonstrates the capability of the developed model in analyzing through as well as buried vias, for which the via current is only partially coupled to the parallel plate mode. The coupling coefficient, β, is trivially dependent on the geometry of the structure [6]-[7]. Thus, for the substrate composed of identical layers shown in Fig. 1, all the β factors are equal.

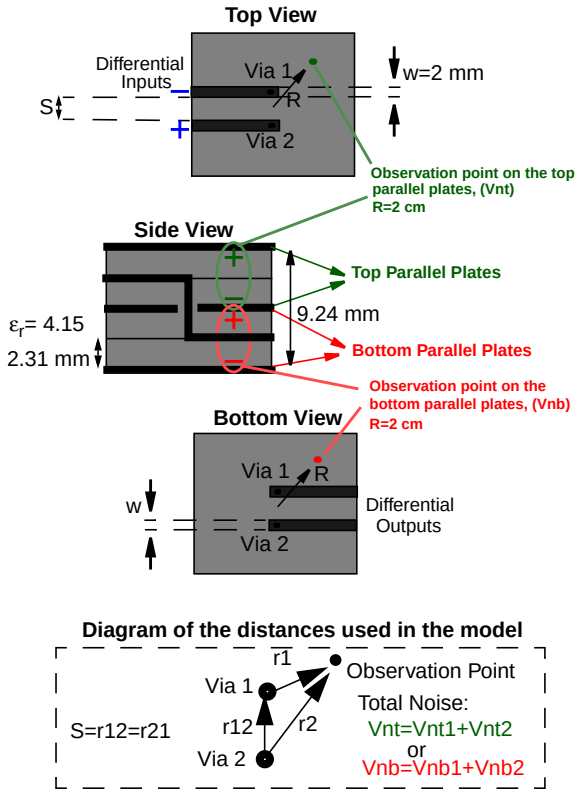

Fig. 1. Multilayer differential via structure.

The proposed model, presented in Fig. 2, comprises two Π equivalent circuits for the two vias but modified to reflect the excitation of the TEM parallel plate mode. The values for Ls and Cs are obtained from fullwave simulation of a single through via-stripline structure. Element C_{x2} models the excess capacitance of the via as well as the parasitic effect of the slot in the middle ground plane (via clearance). The reciprocal induction of the parallel plate mode back to the striplines is included by using the dependent voltage sources βV_{Ct1} and βV_{Ct2}, and βV_{Cb1} and βV_{Cb2} for the top and bottom planes respectively.

As explained in references [6]-[7], in order to predict the voltage difference between the parallel plates for multiple vias, 1-D circuits consisting of two-port admittance networks [Y] and Z terminating impedances are proposed and derived using radial transmission line theory [8]. The [Y] network elements (Y12, Y21,Y1 and Y2), and the terminating impedances (Z(r1), Z(r2), Z(r21) and Z(r12)), in Fig. 2 are calculated using the distance diagram shown at the bottom of Fig. 1. The symbol Z_0 in Fig. 2 stands for the characteristic impedance of the striplines. It should be noted that for simplicity the coupling between the interconnecting striplines has not been included in the model shown in Fig. 2; although this can be easily incorporated based on standard quasi-static coupled-line expressions, if deemed necessary by the given application.

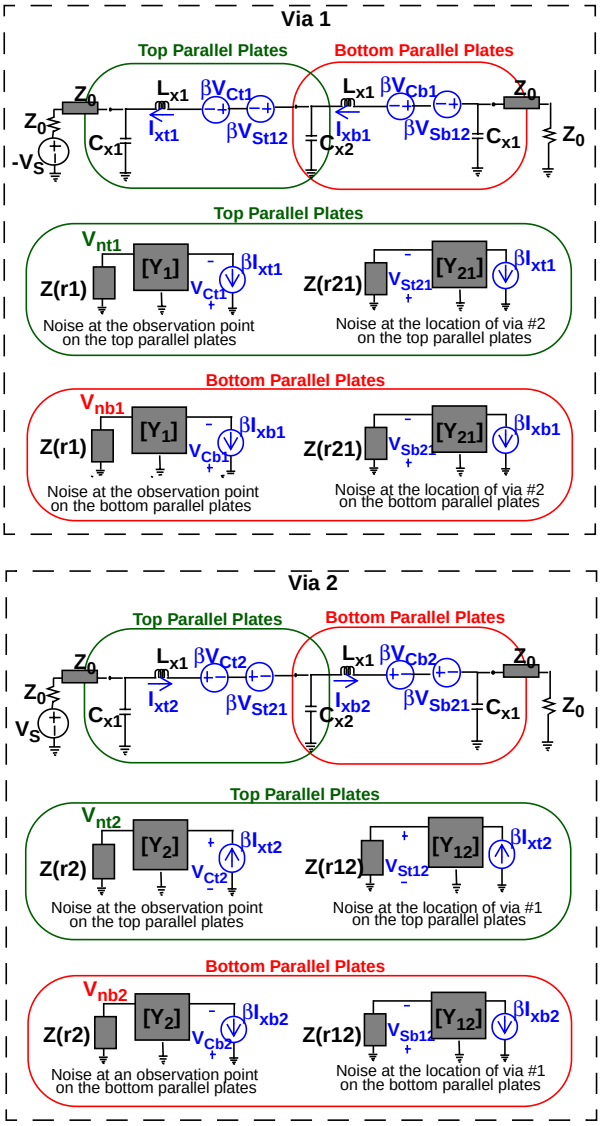

Fig. 2. Proposed equivalent circuit for the differential via configuration of Fig. 1.

Simulations: In order to observe the noise signature on the parallel plates for a differential excitation of the vias, the proposed model was implemented in Agilent-ADS. The

voltage sources are ±2V step functions with a 115 ps (10%-90%) rise time. For Z_0=53 Ω, via diameters of 1mm, line spacing of S=1cm and the observation points at R=2cm on the top and bottom parallel plates, a transient analysis was performed and the results were verified with FDTD as shown in Fig. 3. In the FDTD simulations, vias are conductor strips with 2 mm width and the aperture in the middle plane is a 6 mm x 18 mm rectangle. Note in Fig. 3 that the noise voltage is actually the combination of two parallel plate modes with different delays and opposite phases. The closer via to the observation point generates the stronger noise component due to the shorter delay (r1=1.61cm). The positive noise arrives later (r2=2.44 cm) cancelling part of the negative peak. The magnitude of the noise peak is slightly smaller at the bottom planes because of the relatively smaller current in the part of the via buried in the bottom layer (due to the fringing capacitance of the clearing slot in the middle ground plane). The agreement between the results from the two methods is quite evident in Fig. 3. However, the simulation times were dramatically different, 33 seconds for the proposed model and about 7 hours for FDTD simulations on an Ultra 5 SUN workstation.

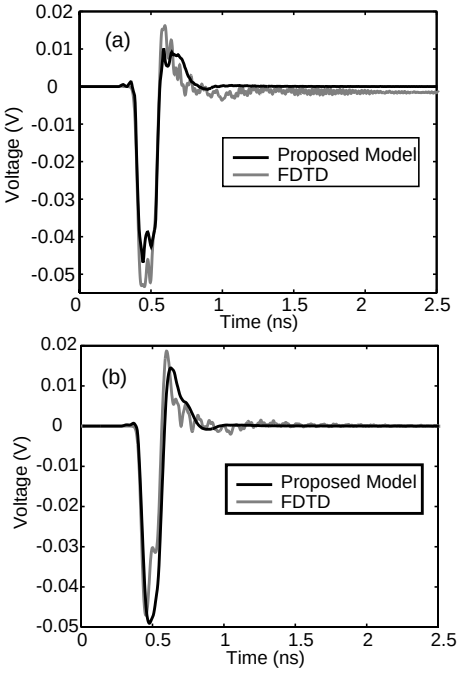

Fig. 3. Noise voltage between the parallel plates for differential vias, S= 1 cm and R=2 cm (a) Top planes, (b) Bottom planes.

Next, the differential via-stripline structures were simulated for a closer spacing, S=4 mm, and the results are shown in Fig. 4. It can be observed that in this case the noise peaks are smaller compared to those of Fig. 3 because the delays for the opposite phase parallel plate modes are now comparable (r1=1.8 cm and r2=2.2 cm).

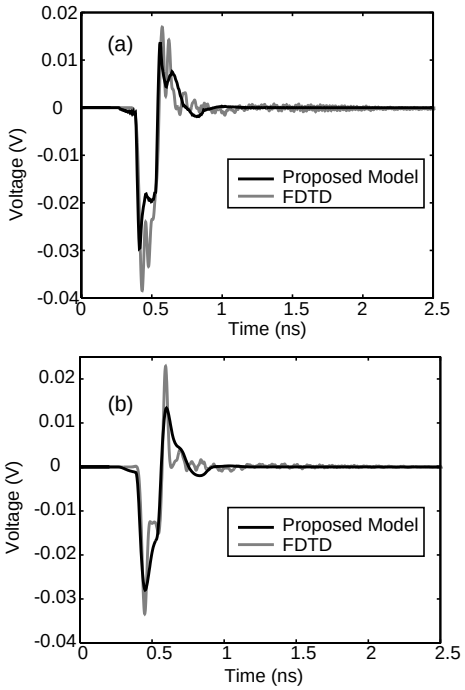

Fig. 4. Noise voltage between the parallel plates for differential vias, S= 4 mm and R=2 cm (a) Top planes, (b) Bottom planes.

III. TDR MEASUREMENTS

Test structure: For the measurements, the test structure shown in Fig. 5(a) was fabricated. The through vias, each located 2mm away from the centre of the board, have a 4 mm spacing. An observation probe was placed 2 cm away from the centre of the 10cmx10cm double sided FR-4 board. The pair of active vias is differentially excited by means of a broadband (DC-40 GHz, Weinschel 1534) resistive power splitter and opposite direction feeds as shown in Fig. 5(a). The coupling between the passive via (probe) and the active vias is included in the same manner as for the case of crosstalk analysis in [6].

Measurement and simulation results: Measurements were performed using a TDR set-up, with a 40 ps rise time step excitation. The signal at the input channel of the TDR system is shown in Fig. 5(b). The generated step voltage from the TDR set up is launched to the input port of the power splitter which has $16\frac{2}{3}\,\Omega$ resistances at each port. Because of the resistive voltage divider used in the power splitter, only 1/2 of the incident signal reaches the coaxial cables feeding the through vias in the parallel plates. The reflected signals from the through vias propagate back to the power splitter and undergo through multiple voltage

divisions and reflections resulting in the ringing signature shown in Fig. 5(b). The rounded corners of the rising and falling edges of the measured signal are due to the dispersion in the coaxial cables which was not accounted for in the simulations.

The noise voltage detected by the output probe, shown in Fig. 5(c), is the superposition of the parallel plate modes excited by each of the two differential vias having opposite signs and almost the same amplitudes. Due to the relatively similar distances between each of the active vias and the probe, 2.13cm and 1.86cm respectively, the resulting noise is quite low validating the noise cancellation capability of closely spaced differential vias. It should be mentioned that the corresponding Agilent-ADS simulations using our developed model for the structure under test, require only 36 seconds on an Ultra 5 SUN workstation and exhibit excellent agreement with the measurements both for the prediction of the input signal as well as for the output noise.

IV. CONCLUSIONS

A physics-based lumped element model for differential vias in a multilayer parallel plate environment has been proposed. The developed model can be incorporated in microwave circuit-simulators such as Agilent-ADS, and results in extremely short simulation times compared to FDTD while maintaining a similar level of accuracy. Different kinds of vias such as, through, buried and blind vias can be treated with this modeling technique. The developed model is an efficient tool for parametric study of differential vias in a parallel plate environment. The results from simulations and measurements presented herein demonstrate that differential vias exhibit a desirable electrical performance in terms of suppressing the TEM parallel plate mode.

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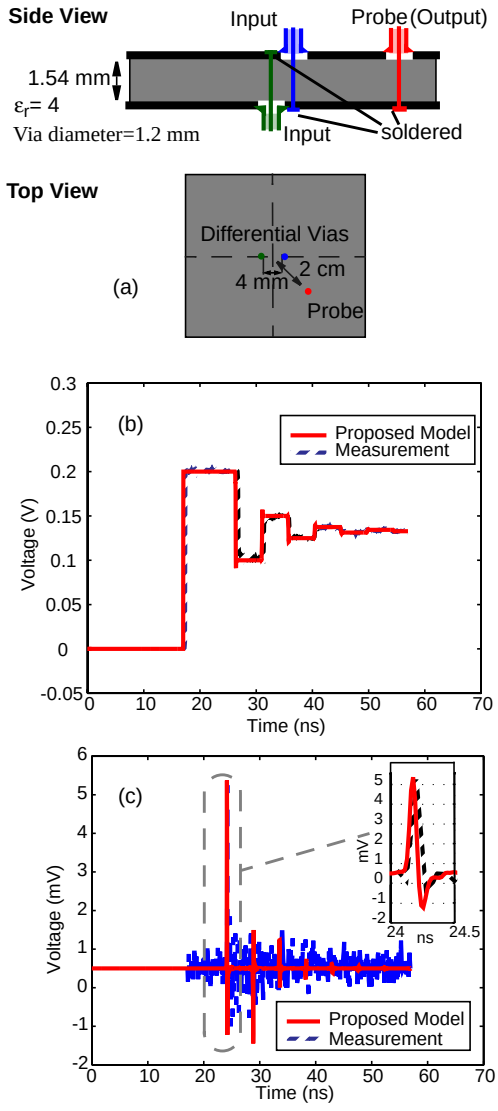

Fig. 5. (a) Diagram of the test structure, (b) Signal at the input port of the power splitter, (c) Probed noise voltage between the parallel plates, R=2 cm.