EMI-INDUCED DELAYS IN DIGITAL CIRCUITS : PREDICTION[1]

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Abstract

A simple model is introduced to predict the changes in propagation delay in a logic inverter caused by low-level radio frequency interference. The change in delay is computed as a function of the induced voltage disturbance, which in turn can be computed from the incident field using linear frequency domain analysis. The model accounts for the dependence of the induced delay on the phase and amplitude of the RFI signal as well as on the slew rate of the logic transitions. Its predictions are shown to be in good agreement with experimental results and Spice simulations for interference frequencies up to the maximum switching frequency of the inverter (in-band interference).

1. INTRODUCTION

When radio-frequency fields are coupled to digital circuits, the resulting radio-frequency interference (RFI) signal causes changes in the propagation delay of the circuit components. It was found by Eprath and Weiner [1] that this effect can lead to failures in digital systems if the changes in delay cause the system timing requirements to be violated.

The delay induction mechanism has been investigated at the single gate level by Alkalay and Weiner [2, 3] and by Tront [4] using the SPICE circuit simulator. Experimental work on MOS devices by Roach [5] and Kenneally *et al.* [6, 7] indicates that the susceptibility to RFI is higher when the RFI frequency is smaller or not too far above the maximum switching frequency of the devices. However, the link between the observed susceptibility and the RFI-induced delays was not explored.

In [2-4], the amount of induced delay is predicted with SPICE, using micromodels that have a large number of parameters for each gate. This approach is not practical for the analysis of a large and complex digital circuit because it requires considerable computer resources. Also, accurate micromodels are not available for many digital devices.

In this paper, we present a simplified method to calculate the amount of RFI-induced delay in logic gates. The main advantage of this model is that the amplitude and phase of the interference signal coupled into the circuit are computed while the logic signals are in a steady state. Extensive simulations have shown that for a fixed logic state, low-level RFI signals can be computed with good accuracy using linear frequency domain analysis [8]. Because of the simplicity of the analysis in the linear regime, digital systems comprising a large number of components can be handled. Furthermore, digital devices can be characterized by their small-signal parameters, which are easily obtained from small-signal measurements.

Section 2 gives experimental results that characterize the changes in the propagation delay of an inverter in the presence of RFI. Then, a model for predicting these changes is developed in Section 3, and its predictions are compared with experimental results in Section 4. The conclusions of the paper are given in Section 5.

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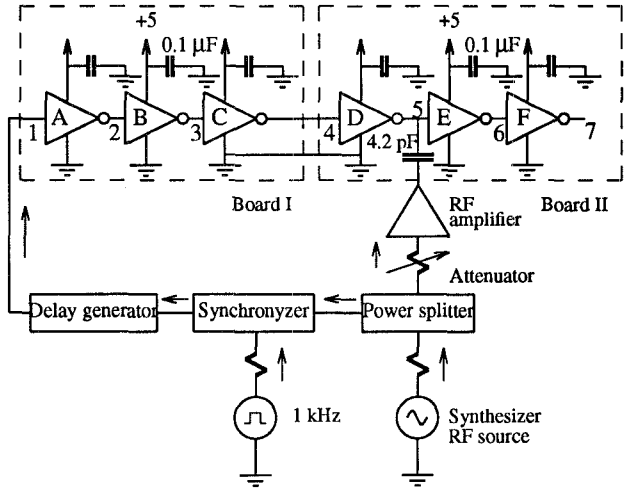
2. MEASUREMENT OF RFI-INDUCED DELAYS

A schematic of the test set-up used to measure RFI-induced delays is shown in Figure 1. It consists of two circuit boards, each carrying three inverter gates on three separate chips. The signals



A, B, C: 4069UB CMOS Hex-inverter
D, E, F: CD4007A CMOS Complementary pair plus inverter

Fig. 1. Experimental setup for measuring RFI-induced delays.

on board I are free from interference and are used as a reference in delay measurements. Board II carries the CMOS inverter chips CD4007A which are the subject of the tests. This particular chip was chosen because of the availability of an accurate gate model developed by Liu [9, 10], which makes it possible to compare experimental and simulation results.

The interference signal is capacitively coupled at node 5 on board II from a 50-Ω RFI source. A synchronizer circuit is used to lock the phase of the RFI signal with respect to the positive edges of the logic pulses sent to the input of the inverter string. With the digital and interference signals synchronized, a variable delay is inserted in the logic signal path to control the time of the switching events within the cycle of the RFI signal. Thus, it is possible to control the phase of the RFI signal at the time of a logic transition.

The time interval between the logic transitions at node 3 and node i (t_{3i}) for i = 5, 6 and 7 was measured. Then, the RFI-induced delay, Δt_i, was computed as

$$\Delta t_i = t_{3i}\text{with RFI} - t_{3i}\text{without RFI}$$

The CMOS devices were powered with a 5-volt supply. Hence, the time of any transition was taken to be the instant at which the voltage crosses the 2.5-volt threshold. Figure 2 shows the induced delay values Δt_5 and Δt_6 as a function of the RFI phase for a 5-MHz 0.63 volt peak-to-peak RFI signal injected at node 5.

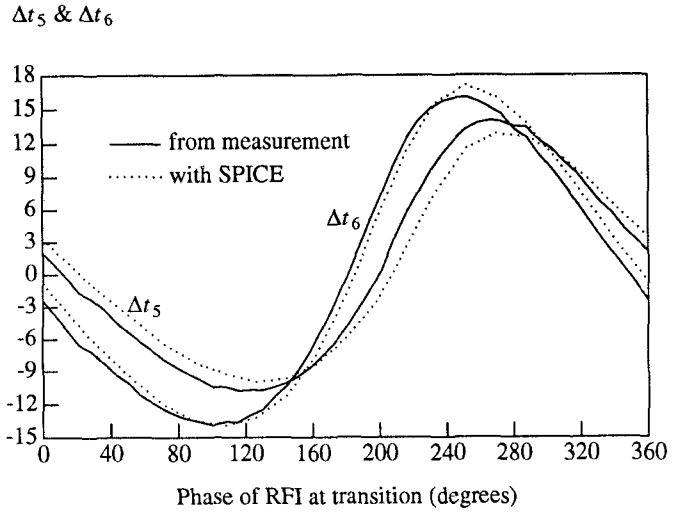


Fig. 2. Extra propagation delay at ports 5 and 6 induced by a 5-MHz, 0.63-volt peak-to-peak intererence capacitively coupled to port 5. The logic transition at port 5 is from low to high.

The RFI amplitude was measured at node 5 while the logic signal at that node was in the low state. The interference frequency of 5 MHz is approximately equal to the maximum switching frequency of the inverters as determined experimentally, and hence constitutes in-band interference. The Δt values obtained from SPICE simulations using the gate models developed by Liu [9] are also shown in the figure and are in good agreement with the experimental results. The notion of phase dependence of the induced delay has been suggested by Tront [4], but it has not been studied experimentally before.

Figure 2 shows that a delay of about 18 ns is caused by an RFI amplitude of only 0.315 volt. For the CMOS device tested, 18 ns is half the propagation delay of the interference-free inverter gate and 0.315 volt is at least four times smaller than the noise margin of 1.45 volt. This means that the failure likelihood associated with RFI-induced delays is an important factor in the EMI immunity of digital circuits.

3. Delay Prediction with Simplified Gate Model

The simulation results in Figure 2 show that a full micromodel for a logic gate can be used to predict RFI-induced delay. However, such models are too complex for the simulation of full scale digital systems. In the following, we present a simple gate model that enables the prediction of RFI-induced delays with sufficient accuracy for the purposes of design and analysis of digital systems.

A. Simplified Inverter Gate Model

A simplified model for a logic inverter gate is shown in Figure 3. The output stage consists of a voltage-controlled current source whose output current I is a function of the internal voltage V and the gate's output voltage V_{out}. The response of the current source is approximated by the piece-wise linear function in Figure 4. The current source's characteristic switches between the upper and lower curves as V crosses the switching threshold of the gate (2.5 volts).

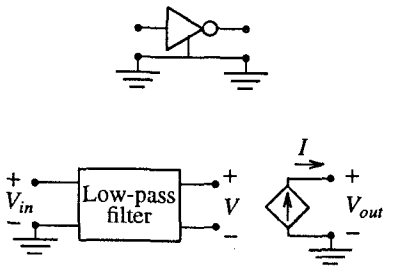


Fig. 3. Simplified model for an inverter gate.

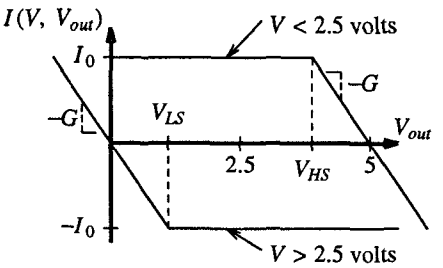


Fig. 4. Response of the voltage-controlled current source as a function of V and V_{out} in the output stage of the simplified inverter model.

Consider now the two-inverter circuit of Figure 5 which is a part of the six-inverter string of Figure 1. Capacitors have been added to represent the wiring and chip packages. The waveforms

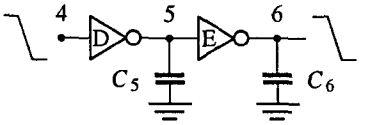


Fig. 5. Two-inverter string with loading capacitors.

for a low-to-high transition at node 5 are illustrated in Figure 6. Before a transition begins at node 5, $V_5 = 0$, $V_6 = 5$ V, and accor-

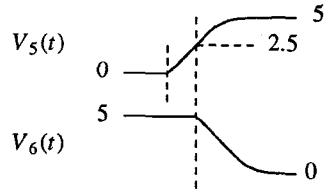


Fig. 6. Voltage waveforms at nodes 5 and 6 in Figure 5 for the gate model of Figures 3 and 4.

-ding to the upper curve in Figure 4 the output admittance of gate E is equal to G ($I_{out} = -I$). As V_5 rises, the output current of gate

6 remains equal to 0, hence V_6 remains equal to 5 V, until V_5 increases above 2.5 V. At this point, the $I - V_{out}$ characteristic of gate E's output switches from the upper to the lower curve in Figure 4. After switching, gate E behaves like a zero-admittance current source, with an output current of $-I_0$. This causes the voltage on C_6 to decrease linearly with time with a slew rate of I_0/C_6, until it reaches V_{LS}. Below this value, V_6 decays exponentially with a time constant of C_6/G.

The simplified gate model in Figures 3 and 4 does not take into account fully the dynamic behavior of the gate. An important feature not predicted by this model is that the slew rate at the output is influenced by the slew rate at the gate's input. Figure 7 gives the measured slew rate S_6 of a high-to-low transition at the

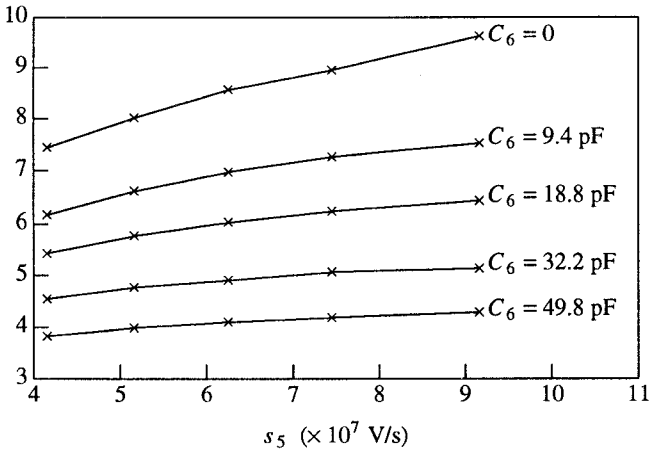


Fig. 7. Slew rate at the output of the inverter gate (s_6) as a function of the slew rate at the gate input (s_5) for different values of load capacitors.

output of the inverter as a function of the slew rate S_5 at its input, for different values of load capacitance. The figure shows that there is an approximately linear relationship between S_5 and S_6. This effect can be accounted for in the model of Figure 4 by making the output current I_0 dependent on the slew rate at the input of the gate.

B. Delay Formula for Low-Level Low Frequency RFI

Consider now the case of an inverter string in which one of the nodes is perturbed with a sinusoidal current source ΔI as in Figure 8, where ΔI is given by

$$\Delta I = \Delta I_0 \sin(\omega t + \phi)$$

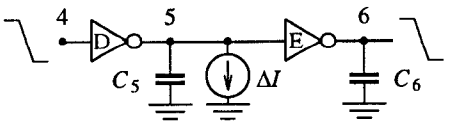


Fig. 8. Two-inverter string with loading capacitors and a disturbing sinusoidal current source ΔI.

At very low interference frequency, the period of the sinusoidal signal is much larger than the duration of logic transitions; hence we can assume that the disturbance current is constant during a logic transition. Let $t = 0$ be the time at which V_4 crosses the 2.5-volt switching threshold during a high-to-low transition. For $t < 0$ and the current disturbance specified above, V_5 is approximately equal to

$$V_5 = \Delta V = \frac{-\Delta I}{G}$$

assuming that $\omega C_5 \ll G$. The voltage waveforms at nodes 5 and 6 are shown in Figure 9 for $t > 0$. If we assume that ΔI is constant

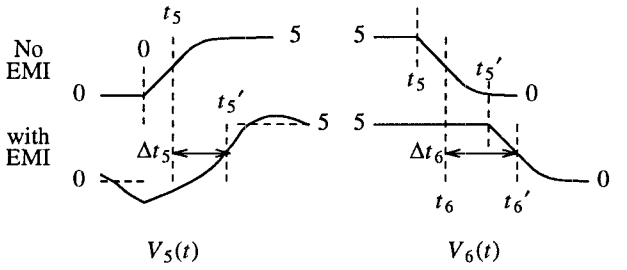


Fig. 9. Typical voltage waveforms for the circuit of Figure 8 in the case of a low-to-high transition at node 5. The waveforms are shown with and without application of disturbance.

during the transition, the time at which V_5 reaches the switching threshold of 2.5 volts (t_5') is given by

$$t_5' = \frac{(2.5 - \Delta V(0))C_5}{I_0 + G\Delta V(0)}$$

In the absence of interference, the 2.5-volt crossing is at $t = t_5 = 2.5\, C_5/I_0$. The RFI-induced delay at node 5 is therefore given by

$$\Delta t_5 = t_5' - t_5 = \frac{(2.5 - \Delta V(0))C_5}{I_0 + G\Delta V(0)} - \frac{2.5\, C_5}{I_0} \qquad (1)$$

The injection of a constant current offset at node 5 causes a slew rate change Δs_5 of:

$$\Delta s_5 = \frac{-\Delta I(0)}{C_5}$$

which in turn causes a change in the output slew rate s_6 given by

$$\Delta s_6 = \frac{\Delta I_6}{C_6} = \frac{\alpha \Delta s_5}{C_6}$$

where ΔI_6 is the change in the output gate current due to the change in s_5 and α is a positive constant. If we neglect the effect of the input filter in Figure 3, the voltage at node 6 begins to change when V_5 reaches 2.5 V. Hence, V_6 will cross the 2.5-volt threshold at t_6' given by

$$t_6' = \frac{2.5C_6}{I_0 + \alpha \Delta s_5} + t_5'$$

Without interference, we would obtain

$$t_6 = \frac{2.5C_6}{I_0} + t_5$$

The extra delay at node 6 is given by $t_6' - t_6$, which after substitution from eq. 1 yields

$$\Delta t_6 = \frac{2.5 - \Delta V(0)}{s_5\left[1 + \frac{G\Delta V(0)}{I_0}\right]} - \frac{2.5}{s_5} + \frac{2.5}{s_6\left[1 + \frac{\alpha G \Delta V(0)}{C_5 I_0}\right]} - \frac{2.5}{s_6} \qquad (2)$$

where $s_5 = I_0/C_5$ and $s_6 = I_0/C_6$. For low-amplitude low-frequency interference, $|G\Delta V/I_0| \ll 1$ and $|\alpha G\Delta V/C_5 I_0| \ll 1$. Hence, eq. (2) can be rewritten as

$$\Delta t_6 \approx -\frac{G\Delta V(0)}{s_5}(1/G + 2.5/I_0) - \frac{G\Delta V(0)}{s_6}\frac{2.5\alpha}{C_5 I_0} \qquad (3)$$

where only the first order terms in $\Delta V(0)$, the pre-transition voltage offset, have been kept. We can rewrite this equation as:

$$\Delta t_6 \approx \Delta V(0)\left[\frac{A}{s_5} + \frac{B}{s_6}\right] \qquad (4)$$

where $A = -(1 + 2.5G/I_0)$ and $B = -2.5G\alpha/C_5 I_0$. Since $\Delta V(0)$ depends on the phase of the interference source, so will Δt_6. Equations (3) and (4) indicate that the extra propagation delay at the output of the gate increases as the slew rates at the input and output ports, measured in absence of interference, decrease.

4. Verification of Delay Predictions for a CMOS Inverter

The results of the previous section were verified using the experimental set-up described in Section 2. In this set-up the output of gate D and the input of gate E are at the same voltage, and the impedance of the 4.2-pF coupling capacitor at the interference frequency of 5 MHz is very large. Therefore, the situation is similar to the case of current source excitation depicted in Figure 8.

A. Effect of RFI Phase on Delays

Experimental results pertaining to the effect of RFI phase on the induced delays were presented in Section 2 (see Figure 2). By comparing eqs. (1) and (2), it can be verified that the minimum and maximum Δt values should be larger in magnitude at node 6 than at node 5. This is in agreement with the experimental results in Figure 2. In general, the experiments showed that for frequencies smaller than 5 MHz, the extrema of Δt_6 were always larger than the extrema of Δt_5. As the frequency is increased above 5 MHz, the opposite behavior was obtained. The discrepancy between this high-frequency behavior and the predictions of eqs. (1) and (2) is partly due to the fact that the effect of the low-pass filter in Figure 3 was not taken into account in the derivation of eqs. (2-4).

Equation (4) was derived for low-amplitude RFI, and only first order terms were retained. Due to this simplification, eq. (4) predicts an induced delay Δt_6 that is proportional to the voltage offset $\Delta V(0)$, which means that Δt_6 is also a sinusoidal function of the phase angle ϕ. The lack of symmetry with respect to the $\Delta t_6 = 0$ baseline in Figure 2 indicates that the RFI amplitude used in the test is outside the range in which the approximation leading to eq. (4) is valid.

B. Experimental Verification of the Amplitude Dependence

Eq. (4) predicts a linear relationship between Δt_6 and the amplitude of the interference signal. The minimum and maximum measured values of Δt_6 for a low-to-high transition at node 5 are plotted in Figure 10 versus the peak-to-peak RFI voltage V_{pp} at different frequencies. For $V_{pp} < 1$ volt, it can be seen that $\max(\Delta t_6)$ and $\min(\Delta t_6)$ are proportional to V_{pp}. The fact that $\max(\Delta t_6)$ and $\min(\Delta t_6)$ have different magnitudes is due to the nonlinear relationship between Δt and ΔV (eqs. (1) and (2)). Figure 10 also shows the diminution of the induced delay as the frequency is increased above the maximum switching frequency of the inverter string (≈ 5 MHz).

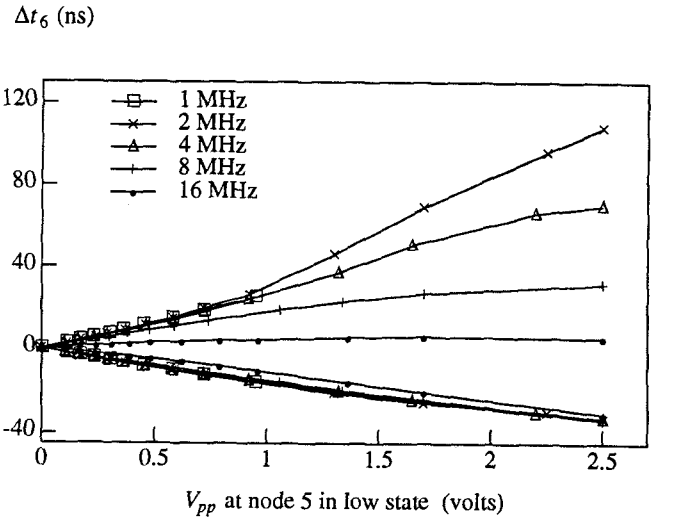


Fig. 10. Measured maximum and minimum RFI-induced delay at node 5 for a low-to-high transition at that node. The interference is capacitively coupled at node 5.

At high frequencies, the period of the RFI signal is comparable to the transition time of the CD4007A, which is about 35 to 40 ns. So, if the disturbing current is maximum at the beginning of the transition, it decreases while the transition is in progress. Therefore, the induced-delay value for an interference signal whose phase is changing rapidly should be smaller than for the case of slowly varying phase. This trend is evident in the experimental results of Figure 10.

C. Experimental Verification of the Slew Rate Dependence

For a given device family and power supply level, the slew rates are only affected by the loading of the gate. If the gate drives a large number of other gates (large fan-out), its output slew rate will decrease. In our test, s_5 and s_6 were controlled by connecting small capacitors of 10, 20, 33 and 47 pF between node 5 and the ground plane and between node 6 and the ground plane. The values of s_5 and s_6 were taken as $3/t_{1-4}$, where t_{1-4} is the time interval between the 1-volt and 4-volt crossings for a 5-volt swing logic transition.

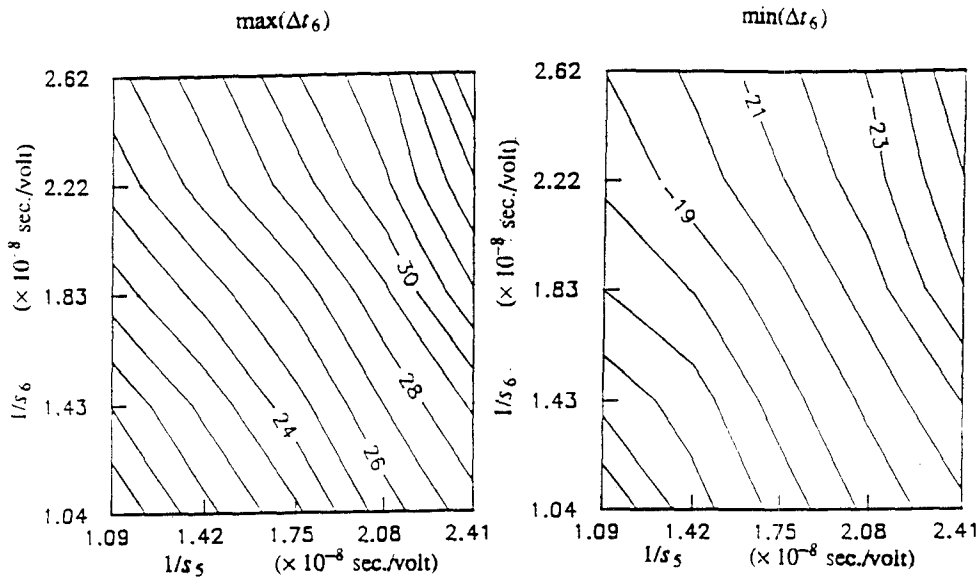


Fig. 11. Maximum and minimum values of SPICE-predicted Δt_6 caused by 1-MHz 0.5-volt-peak-to-peak RFI for different capacitive loading conditions at nodes 5 and 6. s_5 and s_6 are the slew rates at nodes 5 and 6 in absence of RFI. The contour labels are in nanoseconds.

Figure 11 shows contour plots of the maximum and minimum measured values of Δt_6 versus $1/s_5$ and $1/s_6$ for 1-MHz RFI coupled to node 5. For each capacitor value, the RFI source was adjusted to produce a 0.5-volt peak-to-peak signal at node 5 when this node is in the low logic level. It can be seen that the contours are nearly straight and parallel over a large portion of the plane, which means that the worst-case Δt_6 can be approximated by an equation of the form:

$$\Delta t_6 = \frac{a}{s_5} + \frac{b}{s_6} + c \qquad (6)$$

The best-fit a, b and c parameters for the maximum and minimum cases have been estimated by linear regression and are given in Table 1 for a few RFI frequencies, along with the correlation coefficient (r) for each case. Except for the maximum delay at 4 MHz, r is close to 1, which is indicative of a good fit of the experimental data to eq. (6).

Equation (6) has the same form as eq. (4) resulting from the analysis, except for the constant c. The reason for this discrepancy cannot be explained with any degree of certainty because there are too many approximations involved in the derivation of eq. (4).

Figure 10 shows that the worst-case Δt values are almost proportional to the induced RFI voltages for peak-to-peak voltages smaller than 1 volt. This observation may now be combined with the slew rate dependence in eq. (6) to yield the following expression for the worst-case RFI-induced delay

$$\Delta t = \left[\frac{a}{\text{slew}_{in}} + \frac{b}{\text{slew}_{out}} + c \right] v \qquad (7)$$

Table 1. Linear regression coefficients fitting experimental data to eq. (6). s_5 and s_6 are in volts per second and Δt_6 is in seconds.

	frequency (MHz)	a (volt)	b (volt)	c (second)	r
Maximum Δt_6	1	7.67×10^{-1}	5.25×10^{-1}	3.91×10^{-9}	0.991
	2	5.15×10^{-1}	3.40×10^{-1}	9.43×10^{-9}	0.991
	4	9.69×10^{-2}	-5.78×10^{-3}	1.53×10^{-8}	0.566
	8	-3.10×10^{-1}	-2.19×10^{-1}	1.34×10^{-8}	0.884
Minimum Δt_6	1	-5.62×10^{-1}	-3.40×10^{-1}	-3.93×10^{-9}	0.997
	2	-4.68×10^{-1}	-3.01×10^{-1}	-5.26×10^{-9}	0.994
	4	-2.56×10^{-1}	-8.48×10^{-2}	-9.62×10^{-9}	0.936
	8	3.38×10^{-1}	3.28×10^{-1}	-1.75×10^{-8}	0.947

The constants a, b and c are dependent on the RFI frequency and on the polarity of the logic transition. In this expression Δt is the change in propagation delay observed at the gate output due to RFI injected at the gate input, and v is the amplitude of the RFI-induced steady-state voltage at the input of the gate. This formula leads to good approximations for the worst-case delays as long as the disturbance level is in the range where the digital circuit has a linear behavior. For the CD4007A inverter used, this was the case for voltage disturbances not exceeding a peak-to-peak value of 1.5 volt. Constants a, b and c can be plotted versus RFI frequency for each transition polarity. It is suggested that such a plot be included in data books as a part of the performance specifications for each type of logic gate. This information can be used by the designer to improve immunity to RFI, as discussed in [12].

5. Conclusions

In this paper, the change in the propagation delay of a logic circuit caused by radio-frequency interference was studied. The effect of RFI is strongest when the interference frequency is smaller than the gate's maximum switching frequency. The phase and amplitude of the disturbance as well as the slew rate of the logic transitions were found to affect the amount of induced delay. For low-level RFI, the maximum and minimum induced delay are almost proportional to the amplitude of the RFI coupled into the logic signal paths while the circuit is in a quiescent state. Also, the induced delay increases when the slew rate of the logic transitions decreases. These trends have been predicted with a simplified model for the gate, and an expression for the worst-case delays has been derived.

The model presented in this paper does not require the RFI field coupling problem to be solved during a logic transition. The amplitude and phase of the interference signal is needed only while the logic signals are in a steady state. This makes it possible to use linear frequency-domain analysis to compute the parameters of the interference signal.

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References

[1] A. Eprath and D. D. Weiner, "Basic EMC technology advancement for C^3 systems — Probabilistic analysis of combinational circuits with random delays," Rome Air Development Center, Rep. RADC-TR-82-286, Aug. 1984.

[2] J. Alkalay and D. D. Weiner, "Performance degradation of a 7400 TTL NAND gate due to sinusoidal interference," in *1980 Int. Electromagn. Compat. Symp. Rec.*, (Annapolis, MD), pp. 46-51.

[3] J. Alkalay and D.D. Weiner, "Performance degradation of a 7400 TTL NAND gate due to sinusoidal interference," Rome Air Development Center, Rep. RADC-TR-80-257, Aug. 1980.

[4] J. G. Tront, "Predicting URF upset of MOSFET digital IC's," *IEEE Trans. Electromagn. Compat.*, vol. EMC-27, pp. 64-69, May 1985.

[5] J. N. Roach, "The susceptibility of a 1K NMOS memory to conducted electromagnetic interference", in *1981 Electromagn. Compat. Symp. Rec.*, (Boulder, CO), pp. 85-90, Aug. 1981.

[6] D. J. Kenneally, G. O. Head, and C. Anderson, "EMI noise susceptibility of ESD protect buffers in selected MOS devices," in *1985 Int. Electromagn. Compat. Symp. Rec.*, (Wakefield, MA), pp. 251-261, Aug. 1985.

[7] D. J. Kenneally, D. S. Koellen, and S. Epshtein, "RF upset susceptibilities of CMOS and low power Shottky D-type flip-flops," in *1989 Int. Electromagn. Compat. Symp. Rec.*, (Denver, CO), pp. 190-195, May 1989.

[8] J.-J. Laurin, "EMI-induced failures in digital systems," Ph.D. dissertation, University of Toronto, Toronto, Ontario, 1991.

[9] K. Liu, "Modeling of complementary-metal-oxide-semiconductor gates for radio-frequency interference analysis," Ph. D. dissertation, State Univ. of New York at Buffalo, Buffalo, NY, 1988.

[10] K. Liu and J. J. Whalen, "Electromagnetic interference in CMOS circuits," in *1988 Int. Electromagn. Compat. Symp. Rec.*, (Seattle, WA), pp. 471-472.

[11] C. R. Paul, "Frequency response of multiconductor transmission lines illuminated by an electromagnetic field," *IEEE Trans. Electromagn. Compat.*, vol. EMC-18, pp. 183-190, Nov. 1976.

[12] J. Chappel and S.G. Zaky, "EMI-induced delays in digital circuits : application," *Proc. 1992 IEEE Int. Symp. Electromagn. Compat.*, Anaheim, Calif.