Prediction of Delays Induced by In-Band RFI in CMOS Inverters

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***Abstract*— Delays induced by radio frequency interference (RFI) in CMOS inverters are measured under radiated and capacitively coupled interference. Experimental and theoretical investigations of the effects of the RFI coupling mode (capacitive versus inductive) on the amount of induced delay are presented and a worst-case coupling mode is identified. A formula to predict delays caused by in-band low-level RFI in CMOS inverters is introduced. This formula uses experimentally determined parameters which are dependent on the coupling mode. The change in delay is computed as a function of the induced voltage disturbance, which in turn can be computed from the incident field using linear frequency-domain analysis. The formula accounts for the dependence of the induced delay on the phase and amplitude of the RFI signal as well as on the slew rate of the logic transitions. A delay growth phenomenon in a string of inverters is identified and characterized. A correction to the delay prediction formula is proposed in order to take this growth into account in worst-case predictions.**

I. Introduction

THE problem addressed in this paper is the prediction of RFI induced delays in digital circuits. Such predictions are difficult to make due to the large number of components involved in a typical circuit and to a greater extent, to the nonlinear nature of the components' behavior. Therefore, in order to treat practical circuits, simplified models that predict the components' response under RFI excitation should be used. The derivation of such models requires thorough understanding of the phenomena taking place at the gate level. Early work in this area has been carried out by Whalen *et al.* [1] who studied the dc offsets in the output level of NAND gates caused by rectification of high-frequency interference. In Whalen's work, the relationship between the dc rectification and the change in the propagation delay of logic gates, which leads to violation of the timing constraints in digital systems, was not established. The latter effect is expected to be more important in practice, because it occurs at interference levels that are lower than those required to cause dc offsets. Also, timing issues become more crucial to system reliability as clock speeds increase.

The induction of delay by RFI was studied at the gate level [2]–[7] and a method to predict the effects of induced delays at the system level was described in [8]. At the gate level, the circuit considered in most studies is a string of cascaded inverters or buffers. In [2]–[5], the delays caused by in-band and out-of-band RFI are predicted with SPICE using nonlinear micromodels that have a large number of parameters for each gate. This approach is useful to provide insight into the origin of the delay but it is not practical for the analysis of circuits containing large numbers of gates. This is because typical circuits contain numerous devices for which the micromodel parameters are not available. Also, the simulation of such circuits requires considerable computer resources since the models are nonlinear and the simulation has to be done in the time domain.

In [5], we have proposed an alternative to this approach by which the circuit can be simulated in the linear frequency-domain regime. This allows the treatment of large circuits and makes it possible to use frequency-domain analysis programs for solving the field-to-wire coupling problem [9]. Our approach is based on the use of empirical constants obtained experimentally with interference directly coupled to the ports of the inverter. The constants are used in a formula that relates the amplitude of the steady-state voltage disturbance at the input port of the inverter to the RFI-induced delay. Our objective in this paper is to determine under which conditions the formula proposed in [5] can be applied to predict the worst-case induced delays in a typical digital circuit. Mostly in-band effects have been considered in this work. In a number of experimental studies on logic devices, it has been observed that RFI susceptibility is higher when the RFI frequency is smaller than or not too far above the maximum switching frequencies of the devices [5], [6], [10]–[12].

In Section II, we will give experimental evidence that supports the aforementioned statement about the greater in-band susceptibility for the case of the CMOS inverter string. This will be done for two types of interference which are: 1) circuit under test (CUT) in a TEM cell, and 2) interference coupled capacitively to the CUT. We will also briefly summarize the results given in [5] on delay prediction. In Section III, we will examine the influence of the interference coupling mechanism on the inverter's delay. Emphasis will be put on the case of inductive coupling that was not treated in [5]. The objective is to determine the conditions under which the formula derived

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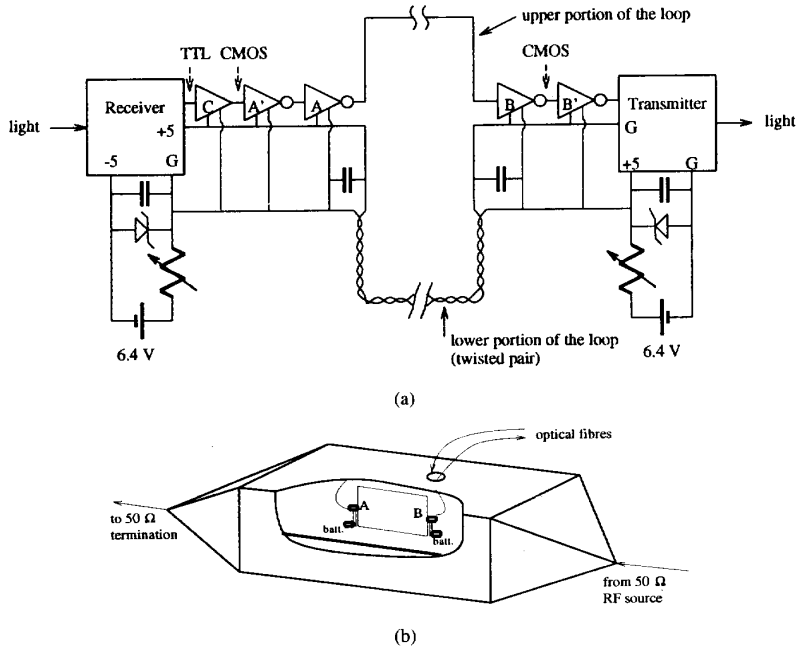

Fig. 1. (a) Details of the circuit under test showing the connections of gates A and B to the square loop. Also shown are the buffer gates A′ and B′, the comparator C, the optical transceivers and the biasing circuit. This drawing is not to scale. (b) Test circuit inside the TEM cell. The two test circuits A and B are connected with a large thin-wire square and are powered with batteries. Digital signals are propagated through the cell wall with optical links.

in [5] can be applied to predict the largest possible delays in a single gate. A correction to this formula, which is applicable only to one inverter, will be given in Section IV to allow the prediction of the delay in an inverter string. With the application of this correction, the prediction of the worst-case delays using a simple linear frequency-domain analysis should be possible.

II. Delay Measurements

A. Delays Induced by Radiated Interference

In [1], [4], [10]–[12], the effect of RFI on digital devices is studied using a 50-Ω RF generator as a source of interference, capacitively coupled to the circuit under test. This method of applying interference allows in-depth study of the devices' failure modes. But, unlike radiated susceptibility tests, it gives no indication on the likelihood of these failures occurring in realistic situations. In practice, the frequency dependence of a circuit's immunity to RFI comes from the frequency response of the devices themselves as well as from the efficiency of the circuit's wiring to pick-up the disturbing fields. This second factor cannot be investigated easily due to the great variability of the wiring geometry. A wiring geometry that is of great interest to the EMC community is the formation of a loop in the link between a driver and a receiver. Such a loop can occur due to poor printed circuit board (PCB) layout or poor grounding between adjacent PCB's. In order to assess the effect of radiated interference on a loop-loaded circuit, we measured induced logic circuit delays by applying a 10 V/m field to a logic circuit in a TEM cell. Optical links were used to carry the signals in and out of the cell, and two 6-volt batteries provided power to the CUT. The CUT, shown in Fig. 1, contains optical TTL transceivers, a comparator (C) to convert the TTL levels to CMOS-compatible 0–5 volt levels, and four cascaded CMOS inverters labeled A', A, B, and B'. The inverter chips were RCA CD4007A. These were chosen because of the availability of an accurate gate model developed by Liu [13], [14], which makes possible the comparison of experimental and simulation results. Inverters A' and B' are used to minimize RFI propagation to the optical transceivers. Inverters A and B are connected with a transmission line whose wire spacing has been exaggerated to form a 29 cm × 29 cm square loop.

The circuit was placed in the center of the TEM cell such that the plane of the loop is parallel to the direction of wave propagation and the loop's normal is parallel to the septum. During the test, logic transitions, which are generated outside the cell, enter the cell as an optical signal, go through the CUT and then come out of the cell again as an optical signal. To evaluate the effect of interference, the propagation delay between the logic transitions of entering and exiting signals is measured with and without an RF signal applied to the cell. The average of the applied electric field along a straight path, normal to the septum and going from the geometrical center of the septum to the cell's outer conductor, is 10 V/m. The RFI signal is synchronized with the transitions of the logic signal (as will be described in Section II-B) to investigate the effects of the RFI phase on delays.

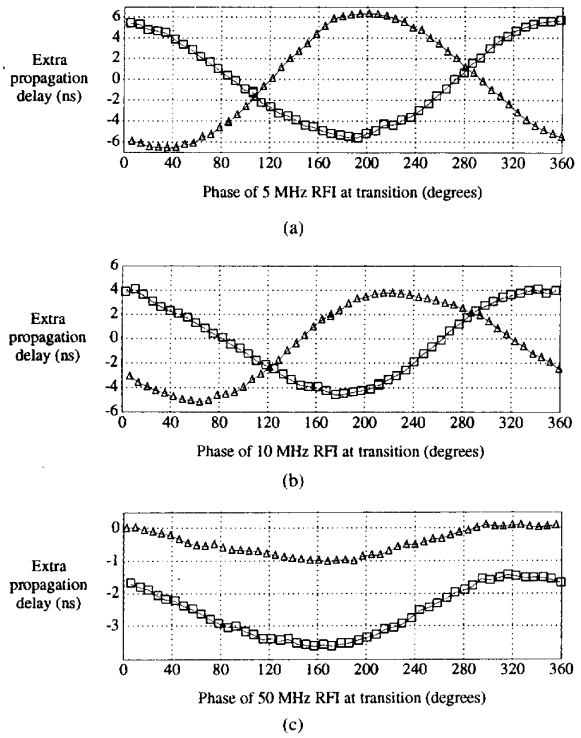

Fig. 2. Extra propagation delay of the TEM-cell circuit for an incident field having a 10 V/m amplitude and (a) 5, (b) 10, and (c) 50 MHz frequencies. □ stands for low-to-high transition and △ for high-to-low transition at the input of gate B.

The RFI-induced delay is defined as

$$\Delta t = t_w - t_{w/o}$$

where t_w and $t_{w/o}$ are the propagation delays with and without the interference field. Fig. 2 shows the delays measured at various phases of the incident field for three RFI frequencies. At 5 MHz, the RFI frequency is approximately equal to the maximum switching frequency of the CD4007A inverters as determined experimentally, and hence constitutes in-band interference. It is at this frequency that the highest value of Δt was obtained (about 6 ns). As the frequency increases, the inductive coupling in the loop should lead to an increased level of RFI voltage at the terminals of gates A and B. However, the results show a decrease of Δt at higher frequencies, indicating that induced delays have a higher probability of occurrence, and a greater likelihood to cause failures, for in-band RFI.

The dependence of Δt on the phase of the RFI signal changes as frequency increases. At 5 MHz, the Δt-versus-phase curve is nearly symmetric about the $\Delta t = 0$ line, whereas the same curve at 50 MHz consists of a constant negative term superimposed on a small phase-dependent contribution. The notion of phase dependence of the induced delay has been briefly discussed by Tront [4] for out-of-band interference, but it has not been studied experimentally before. The existence of a significant phase-independent contribution at high frequencies suggests that the delay induction mechanism is different than for in-band frequencies. Possibly, dc rectification of the RFI signal [1] might be responsible for this effect.

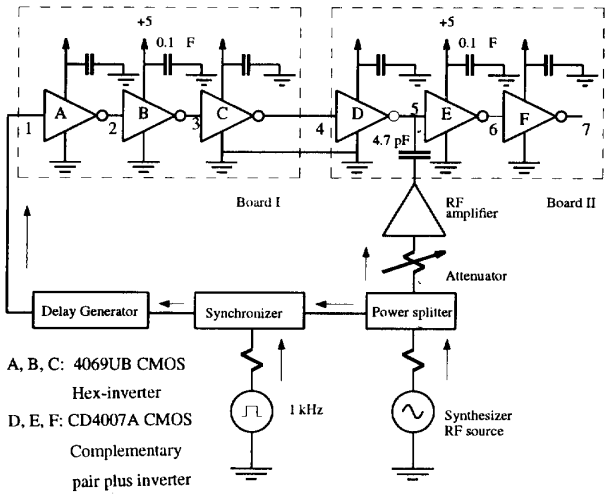

Fig. 3. Experimental setup for measuring RFI-induced delays.

B. Capacitively Coupled Interference

The induced delays were also measured with a string of inverters mounted on a board using microstrip lines, and interference was coupled to the circuit through a capacitor. A schematic of this set-up is shown in Fig. 3. Unlike the case of the TEM cell test, this set-up allows almost disturbance-free measurement of the voltage waveforms at various circuit nodes using high-impedance probes. The CUT consists of two circuit boards, each carrying three inverter gates on three separate chips. The signals on board I are free from interference and are used as a reference in delay measurements. Board II carries the CMOS inverter chips which are the subject of the tests.

The interference signal is capacitively coupled at node 5 on board II from a 50-Ω RFI source. A synchronizer circuit is used to lock the phase of the RFI signal with respect to the positive edges of the logic pulses sent to the input of the inverter string. With the digital and interference signals synchronized, a variable delay is inserted in the logic signal path to control the time of the switching events within the cycle of the RFI signal.

Figs. 4 and 5 show digitized waveforms of the logic signals recorded at nodes 3, 5, and 7 with and without interference. The two figures correspond to RFI frequencies of 5 and 50 MHz, respectively. The effect of interference is not visible on the waveform of V_3. At node 5, where the RFI signal is injected, very mild perturbations can be seen in the 0 and 1 states for the 5 MHz interference. The perturbations cause a change of slope combined with a shift of the waveforms during the logic transitions. Due to these effects, the time at which V_5 crosses the 2.5-volt logic threshold changes when interference is present. At 50 MHz, V_5 crosses the 2.5-volt threshold a number of times for each logic transition of the V_3 waveform. The average level of V_5 during the steady 0 and 1 states is shifted to a value greater than 0 during the low state

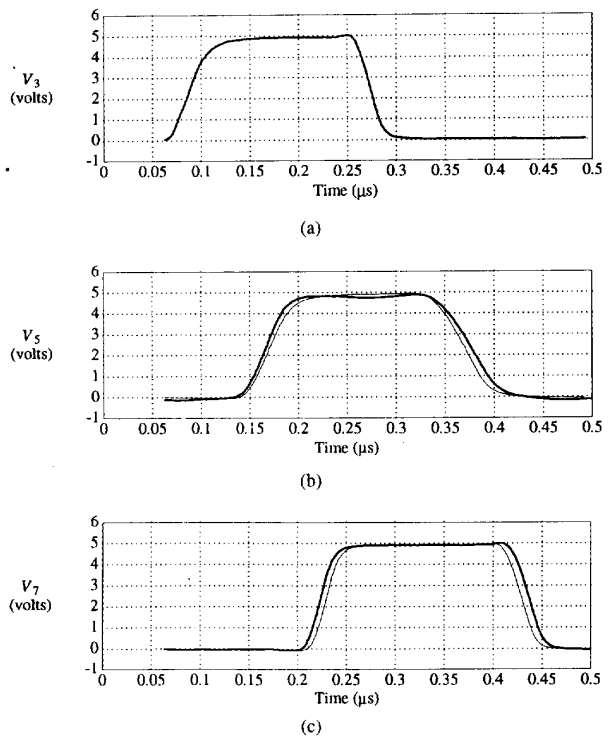

Fig. 4. Measured voltage waveforms at (a) node 3, (b) node 5, and (c) node 7 with weak in-band interference (thick traces) and without interference (thin traces). The RFI frequency is 5 MHz and the incident power is 15 dBm.

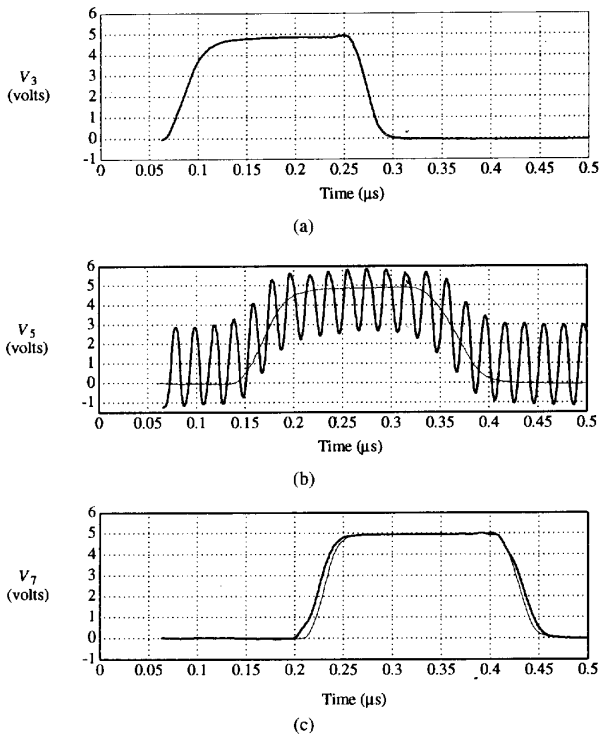

Fig. 5. Measured voltage waveforms at (a) node 3, (b) node 5, and (c) node 7 with strong out-of-band interference (thick traces) and without interference (thin traces). The RFI frequency is 50 MHz and the incident power is 30 dBm.

and smaller that 5 volts during the high state. This is due to the rectification action of the input protection diodes built into CMOS gates. The dc rectification contributes to a reduction of the noise margin, as pointed out by Whalen *et al.* [1]. For both frequencies, the output waveform (V_7) does not show any disturbance in the 0 and 1 states, which is a consequence of the large noise margin of the CMOS technology (1.45 volt). However, it can be clearly seen that the transition disturbances at node 5 have been propagated to the output, and therefore have induced a change in the propagation delay, Δt_7, of the logic transitions at node 7. The incident RF power at 50 MHz is 32 times larger than in the 5 MHz test. However, Δt_7 is of the same order of magnitude in both cases. This indicates that gate susceptibility is higher for in-band RFI, which is consistent with the results of Section II-A and of earlier publications [5], [6], [10]–[12]. For this reason, the rest of this paper will focus on the prediction of delays caused by in-band interference.

Because V_3 is not affected by RFI, logic transitions at node 3 were used as a time reference for induced delay measurements. The time interval t_{3i} between logic transitions at node 3 and node i for $i = 5, 6, 7$ was measured. Then, the RFI-induced delay, Δt_i, was computed as

$$\Delta t_i = t_{3i,w} - t_{3i,w/o}$$

where as before, subscripts w and w/o refer to measurements with and without the interference signal. The CMOS devices were powered from a 5-volt supply. Hence, the time of any transition was taken to be the instant at which the voltage crosses the 2.5-volt switching threshold. Fig. 6 shows the induced delay values Δt_5 and Δt_6 as a function of the RFI phase for a 5-MHz 0.63 volt peak-to-peak RFI signal injected at node 5. This figure was also presented in [5] but it is repeated here in order to support the discussion in the following sections. The RFI amplitude was measured at node 5 while the logic signal at that node was in the low state. The Δt values obtained from SPICE simulations using the gate models developed by Liu [13] are also shown in the figure and are in good agreement with the experimental results.

Fig. 6 shows that a delay of about 18 ns is caused by an RFI amplitude of only 0.315 volt. For the CMOS device tested, 18 ns is half the propagation delay of the interference-free inverter gate and 0.315 volt is at least four times smaller than the noise margin of 1.45 volt. This means that the failure likelihood associated with RFI-induced delays is an important factor in the immunity of digital circuits.

In [5], a model was derived to predict the delay induced in this inverter by in-band RFI. The interference source considered was a current generator applied at the input terminal of the inverter. This is similar to the case depicted in Fig. 3 where RFI is coupled through a high impedance capacitor. In this model, the inverter's output stage is assumed to behave as a passive conductance when the gate is in steady state and as a current source during the logic transitions. Using

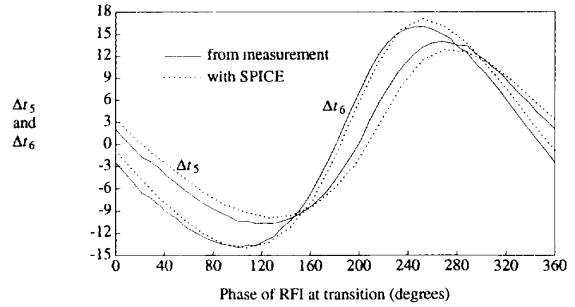

Fig. 6. Extra propagation delay at ports 5 and 6 induced by a 5 MHz, 0.63-V peak-to-peak interference capacitively coupled to port 5. The logic transition at port 5 is from low to high.

this simplified model, we arrived at a formula that gives the delay at the output of the perturbed gate as a function of the amplitude of the steady-state voltage disturbance ΔV at the input of the gate, before the beginning of the logic transition. Experimental results showed good agreement with the predictions of the formula. In particular, it was found that the delay increases linearly with ΔV up to a peak-to-peak value of 1.5 volt. It was also found that the slew rate of the voltage waveforms at the gate's input and output ports during the logic transition, which is greatly dependent on the loading of the circuit, has a direct influence on the delay. In fact, the delay was found to increase, thereby increasing the circuit's susceptibility, as the speed of the transition decreases. A rule of thumb frequently used by PCB designers to reduce the level of emissions is to load the devices with resistors and capacitors to increase the rise and fall times. For the type of CMOS devices used in this work, our results suggest that such a strategy will lead to a greater susceptibility to timing errors.

When the interference is applied with a current generator at the inverter's input port, the delay is related to the voltage disturbance ΔV by the following:

$$\Delta t = \Delta V\left(\frac{a}{\text{slew}_{\text{in}}} + \frac{b}{\text{slew}_{\text{out}}} + c\right). \tag{1}$$

In this equation, parameters a, b, and c can be determined experimentally. The denominators are the slew rates at the gate's input and output measured with no RFI applied to the gate.

III. Effect of Coupling on CMOS Inverter Delay

The case of RFI capacitively coupled to one node of the logic circuit has been covered in Section II-B and in [5]. In this section, we will examine the effect of the coupling mode to determine the conditions leading to the worst-case induced delay. We will also estimate the extent to which the delay induced in one perturbed gate will propagate in a network of gates connected to the output of that gate.

Consider the perturbation of the link between gates D and E in Fig. 3. The output of the driving gate (gate D) will be called port 1 and the input of the driven gate (gate E) will be called port 2. Let us represent the link by a short segment of transmission line. The effect of applied interference on the

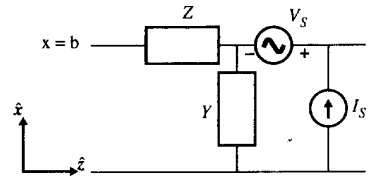

Fig. 7. Per-unit-length model of a transmission line illuminated by incident electric and magnetic fields.

transmission line can be taken into account by augmenting the line model with per-unit-length, distributed voltage and current generators as shown in Fig. 7. These sources are related to the incident electric and magnetic fields via the following equations [15]:

$$V_S(z) = j\omega \int_0^b B_y^i(x, z)\, dx$$

$$I_S(z) = -Y \int_0^b E_x^i(x, z)\, dx$$

where Y is the per-unit-length admittance $(G + j\omega C)$ of the line. If the segment of transmission line is very short electrically, the approximate behavior of the circuit can be obtained by considering a lumped model where the per-unit-length parameters are multiplied by the line's physical length. For the chip considered in this paper, in-band frequencies are smaller than 5 MHz ($\lambda = 60$ m) and it is clear that for typical circuit traces found on PCB's, the line length will be of the order of $\lambda/200$ or less. In this case, the incident fields are approximately included in the model by a current source which accounts for the electric field (capacitive coupling) and a voltage source which accounts for the magnetic field (inductive coupling). If we consider a short segment of transmission line in air exposed to an incident TEM wave propagating in the z direction with $\boldsymbol{E} = E_x\hat{\boldsymbol{x}}$, it is easy to prove that $V_S/I_S = -Z_o$ where Z_o is the characteristic impedance of the line. This situation is somewhat analogous to the TEM cell test described in Section II-A, the difference being the nonuniformity of the fields and the influence of the cell walls on the line's characteristic impedance. Neglecting this last effect, we find that the V_S values corresponding to the 5, 10, and 50 MHz frequencies in Section II-A are respectively 0.17, 0.34, and 1.7 volt. The value for Z_o in this case is approximately 700 Ω [9].

The expression given in the previous section to calculate Δt was derived by assuming capacitive coupling only. It is therefore not complete because inductive effects are not included. An expression for the delay induced by a voltage source can be derived by making the same assumptions as in [5] for the case of capacitive coupling. For in-band interference, the period of the RFI is much longer than the logic transitions. Therefore, we are assuming a constant voltage disturbance in the derivation. The string of two inverters shown in Fig. 8 is perturbed with source V_S and the current I_S is set to zero. In steady state, the output of gate D, assuming a logic value of 0 at node 5′, can be modeled by a conductance G representing the channel of the NMOS transistor in this gate. This conductance is in parallel with a parasitic capacitance C_o, which accounts for extrinsic

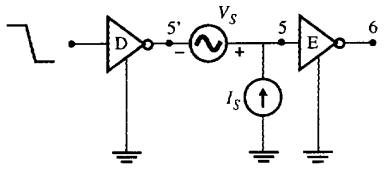

Fig. 8. Electrically short link between two inverters perturbed by incident electric and magnetic fields.

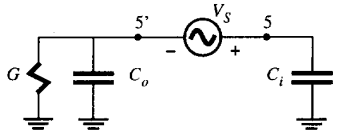

Fig. 9. Small-signal model for the two-inverter string in steady state disturbed with inductively coupled RFI.

and intrinsic charge storage effects. On the other hand, the input stage of gate E is nearly equivalent to a capacitive load C_i. In steady state, the resulting equivalent circuit represented in Fig. 9 yields $V_{5'} = 0$ and $V_5 = -V_S$. When gate D's output is switching from logic 0 to logic 1, the conductance G in the model is replaced by a voltage-dependent current source I_o. Assuming a constant I_o value during the transition, the voltage at node 5 is given by

$$V_5 = -V_S + \frac{I_o}{C_o + C_i}(t - t_o) \tag{2}$$

where t_o is the time at which the transition begins. It should be noted that the voltage disturbance does not affect the slew rate of the V_5 waveform which stays equal to $I_o/(C_o + C_i)$ in the presence of interference. This is the main difference compared with the case of disturbance by a current source where we have both an offset voltage and a change in slew rate [5]. Using (2), we find that the V_5 waveform reaches the switching threshold of 2.5 volts at time $t_{2.5}^{\mathrm{RFI}}$ given by

$$t_{2.5}^{\mathrm{RFI}} = \frac{(2.5 + V_S)}{I_0}(C_o + C_i) + t_o$$

when interference is present and

$$t_{2.5} = \frac{2.5}{I_o}(C_o + C_i) + t_o$$

without interference. This yields an RFI-induced delay of

$$\Delta t_5 = \frac{V_S}{I_o}(C_o + C_i) = -\frac{V_5^{\mathrm{RFI}}}{I_o}(C_i + C_o) \tag{3}$$

where V_5^{RFI} is the magnitude of the steady-state RFI disturbance at node 5 before the transition. In the case of a current source disturbance, the delay expression found in [5] was

$$\Delta t_5 = -V_5^{\mathrm{RFI}} \frac{C_i + C_o}{I_o + GV_5^{\mathrm{RFI}}}\left(1 + \frac{2.5G}{I_o}\right).$$

For positive values of V_5^{RFI}, this expression leads to larger negative delays than (3). As discussed above and in [5], the difference of slew rate which occurs with a current disturbance will also contribute to increase the delay at the output of gate E.

According to the above equations, it follows that for a given level of induced voltage at the input of gate E (V_5^{RFI}), the maximum delay will be obtained with a current source or capacitively coupled interference. However, we have used a simplified gate model and a static assumption for the disturbing source in our derivation. Furthermore, we have not considered the case where I_S and V_S are applied simultaneously. In order to validate our conclusion, we simulated the circuit of Fig. 3 under the two types of disturbance (as in Fig. 8) with SPICE. In practice, the distribution of the incident field on the circuit can be quite complex and the values of I_S and V_S are unpredictable. For this reason, we decided to consider all possible cases in our simulation. This was accomplished by varying four parameters, namely the phase and magnitude of I_S and V_S. For each set $\{|I_S|, \angle I_S, \angle V_S\}$, the magnitude of V_S was adjusted to generate a peak V_5^{RFI} value of 1 volt. In each case, enough time was allowed to let the RF disturbance reach a steady state; then, a logic transition was initiated at the input of gate A. This process was repeated for a few values of $|I_S|$ and in each case, $\angle I_S$ and $\angle V_S$ were varied by 10-degree increments over a span of 360 degrees.

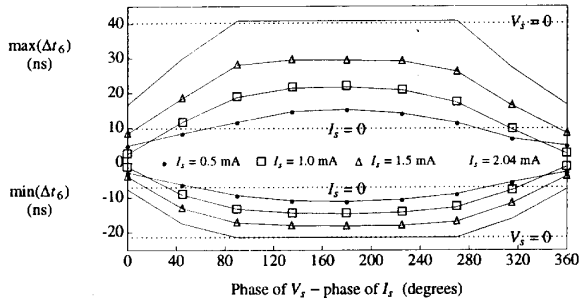

Fig. 10. Extra propagation delay at node 6 induced by a 1-MHz, 1-V peak-to-peak interference coupled to node 5 with various combinations of current and voltage sources. The logic transition at node 5 is from low to high and the interference voltage is measured in the logic-low state. The results were obtained from circuit analysis using SPICE.

The worst delays for various $I_S - V_S$ combinations that yield a 1-volt peak disturbance at port 2 are shown in Fig. 10. These results are for an interference frequency of 1 MHz. In the figure, the solid lines are for fixed I_S amplitudes of 0.5, 1.0, 1.5, and 2.04 mA. The dotted lines at $\Delta t_6 = 40$ ns and $\Delta t_6 = -22$ ns are for pure $|I_S|$ excitation, and those at $\Delta t_6 = 10$ ns and $\Delta t_6 = -8$ ns are for pure V_S excitation. From the figure, it can be seen that the worst-case delays are never greater than those obtained with I_S alone. This is consistent with the result found above with the simplified gate model.

IV. Delay Growth in an Inverter String

Fig. 6 shows that the worst delays measured one gate after the node of injection (Δt_6) are greater than the worst delays at the node of injection (Δt_5). In [5], we have attributed this

TABLE I
GROWTH FACTOR FOR DELAYS THROUGH A STRING OF CASCADED INVERTERS FOR RFI INJECTED AT NODE 5

	Growth factor			
frequency (MHz)	node 6 (%)	node 7 (%)	node 8 (%)	node 9 (%)
1	58.6	78.4	79.3	79.7
2	54.8	71.8	70.7	70.3
4	45.9	58.1	57.8	57.9
8	8.7	3.3	2.0	4.0
16	-85.2	-101.5	-99.7	-98.6

TABLE II
CORRECTION FACTOR FOR DELAY GROWTH THROUGH OUTPUT CIRCUITRY OF CD4007A

frequency (MHz)	correction factor for positive delay	correction factor for negative delay
1	1.13	1.12
2	1.11	1.10
4	1.08	1.08
8	1.96	1.01
16	0.09	0.33

effect to the change of slew rate at the output of gate E caused by an RFI-induced slew rate change at its input. Using the same reasoning, it can be argued that the slew rate change at node 6 will in turn cause a slew rate change at node 7, and so on; that is, the induced delay will keep growing as the logic transition propagates along a string of gates. Therefore, (1) at the end of Section II, which would give the delay at node 6 for a given voltage disturbance at node 5, might not give the maximum possible delay in the inverter string.

In order to estimate the rate of delay growth, a string of 8 inverters was simulated with SPICE. The RFI was coupled capacitively to node 5 as in Fig. 3, and the induced delay at nodes 5 to 9 was calculated using the definition given in Section II for Δt_i. Then, a growth factor GF(n) was calculated according to the formula

$$\mathrm{GF}(n) = \frac{\max(\Delta t_n) - \max(\Delta t_5)}{\max(\Delta t_5)} \times 100.$$

Table I gives the growth factors for several RFI frequencies. The results indicate that the delays stabilize at node 7, that is, two gates after the node of injection. At 1 MHz, the maximum delay is about 80% larger than the delay obtained at the mode of injection. But, as the frequency increases, this growth diminishes, especially for out-of-band RFI. At 16 MHz the growth is nearly -100%, which means that the delay induced at the node of injection has vanished completely at the end of the string. For in-band interference, there is a large difference between the growth at nodes 6 and 7. Therefore, (1) does not predict the worst-case delay. To compensate for the difference between the worst-case delay and the computed Δt_6, a multiplicative correction factor CF(n) can be included in (1) where

$$\mathrm{CF}(n) = \frac{\max(\Delta t_n)}{\Delta t_6} \qquad n > 6.$$

The values of CF(n) for positive and negative delays are given in Table II. This table shows that in the worst case, the positive Δt might be underestimated by 13% if the growth effect is not taken into account.

V. CONCLUSION

The change in the propagation delay of a logic circuit caused by radio-frequency interference was studied. The voltage waveforms at the ports of RFI-perturbed CMOS inverter gates were examined and the induced delays measured. Tests were carried out with capacitively-coupled interference and with radiated interference inside a TEM cell. These measurements confirmed earlier observations that the delay is significantly larger for in-band interference, that is, when the RFI frequency is smaller than the gate's maximum switching frequency. They also showed that the RFI-induced delay depends on the way in which the RFI signal is coupled to the circuit under test.

In the earlier work, an empirical formula was proposed for predicting the induced delay in a single CMOS inverter. The delay is computed based on the value of the RFI-induced RF voltage under steady-state conditions: that is, while the logic signal is in a quiescent state. In this paper, the conditions under which this formula yields worst-case delay have been examined. It has been shown that, for a given induced voltage, worst-case delay occurs when the signal is capacitively coupled. Hence, the constants in the empirical formula must be measured with capacitively coupled interference. Tests conducted in a TEM cell will underestimate the amount of induced delay. It has also been shown that the delay induced in a string of inverters is higher than for a single inverter, even when RFI is injected at only one point. A correction to the original formula has been given to account for this effect.

The main advantage of the delay prediction formula used in this paper is that the induced delay calculation is based on the amplitude of the interference signal while the logic signals are in a quiescent state. Thus, it is not necessary to solve the field coupling problem during the logic transitions where the gate behavior is highly nonlinear. Furthermore, since the gates studied behave almost linearly in the quiescent states, it is possible to use linear frequency-domain analysis to compute the amplitude of the interference signal.

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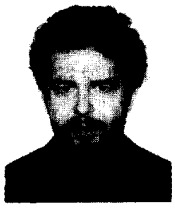

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