# On the Prediction of Digital Circuit Susceptibility to Radiated EMI

Jean-Jacques Laurin, *Member, IEEE,* Safwat G. Zaky, *Member, IEEE,* and Keith G. Balmain, *Fellow, IEEE*

***Abstract*—The effects of radiated radio-frequency interference (RFI) on the operation of digital systems are studied by simulating the response of simple logic circuits to incident plane waves. The simulation is accomplished by combining a linear electromagnetic moment-method model of the wire structure with a nonlinear circuit model of the solid-state components. The complete model is analyzed in the linear and nonlinear regimes as an example. It is shown how a circuit simulator, such as SPICE, can be used in the analysis of an arbitrary wire network loaded with logic circuits, by the process of representing the linear wire network as a lumped-element $N$-port $\pi$ network and interfacing it to the nonlinear circuit simulator. Examples are given that demonstrate the occurrence of both static and dynamic failures under various RFI-field excitations and wire structure geometries. The prediction methods presented in this paper, can be used by emc engineers to assess the likelihood of failures in RFI-exposed digital systems.**

## I. Introduction

OVER THE PAST thirty years we have observed a tremendous increase in the switching speed of components used in digital electronic equipment. As a result, timing issues have become a major factor in logic systems design. Tighter synchronization of logic signals requires better signal integrity, and leaves less room for disturbances such as those induced by electromagnetic interference (EMI). Also, the widespread use of MOS-based instead of bipolar logic families means that careful attention should be paid to susceptibility to EMI. CMOS gates have larger noise margins than TTL gates, which should make them more immune to interference. However, TTL circuits operate at lower impedance levels, and more power is needed to make them fail [1].

A number of authors have reported experimental results on the effect of radio-frequency interference (RFI) on logic gates [1]–[9]. Except for [9], these studies were carried out by injecting an interference signal directly into the input and output ports of digital gates via a capacitor or other lumped devices. Direct injection is useful for several reasons. It makes possible the examination of chip failures using very simple experimental setups. Lumped-element interference coupling is germane to the bulk current-injection method that is now specified in many standard susceptibility test methods. Also, the prediction of logic circuit failures caused by interference coupled through lumped elements is easy to perform with simulators such as SPICE, in which lumped elements having ideal behavior over a wide frequency range are implemented.

In the case of radiated susceptibility, simulation of failures is difficult. While the interference coupling is distributed over the conductor traces forming the circuit, a lumped model of the field-excited conductor structure is needed for use in a circuit simulator. The model should include a network to model the passive conductor structure and signal sources to model the incident field. It should also be valid over a wide frequency range, because logic gates are nonlinear devices that operate in a transient regime. Such broadband models exist and can be analyzed using circuit simulators supporting transmission line models. However, modeling with transmission lines is applicable only when the conductor structure is made of long parallel wires that form multiconductor transmission lines (MTL) [10]. It is less accurate when the structure is irregular in shape as a result of bends and other discontinuities encountered in digital interconnect structures. Furthermore, since the net current through any cross-section transverse to an MTL must be zero according to transmission line theory, MTL-based models cannot predict generation of, or perturbation by, common mode currents.

In this paper, we introduce simulation tools that can be used to calculate the response to radiated interference of digital circuits having a conductor structure of arbitrary shape. The purpose of these simulations is to predict the occurrence of failures induced by radiated EMI. Two specific types of failures will be discussed: static failures and dynamic failures. Static failure occurs as a result of signal excursions that exceed the noise margin of the components. Hence, its prediction requires large signal simulation in the nonlinear regime, as described in Section III. Dynamic failure, on the other hand, is caused by small interference signals that change the timing of logic signal transitions. It can be predicted with linear small-signal analysis, as discussed in Section IV. The methods proposed are based on the use of commercially available simulators for nonlinear semiconductor circuits and a thin-wire moment-method modeling code to analyze field coupling. First, we will report on the use of these tools to investigate the effect of radiated interference on a basic logic circuit, namely a pair of inverters, when the incident field level is

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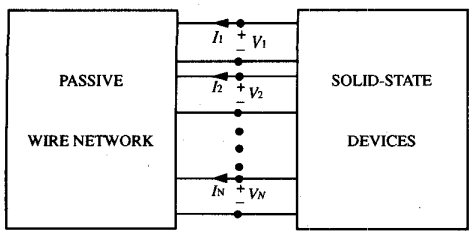



Fig. 1. Model for digital circuit without RFI.

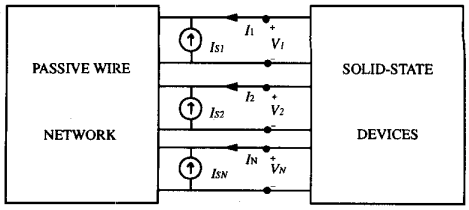



Fig. 2. Digital circuit model including incident RFI field implemented with current sources.

comparable to those specified in EMI standards. Then, we will address the problem of modeling digital systems consisting of a large number of digital components. Only continuous radio-frequency interference (RFI) will be considered.

## II. Equivalent Network for Field-Exposed Circuits

In this section, we will consider the modeling of a digital circuit made of conducting traces loaded with solid-state components. The integrated circuits (IC's) are assumed to be much smaller in size than the features of the trace structure, and also much smaller than the wavelength of the incident RFI field. In this case, it is possible to consider each IC as a lumped device having all its terminals at infinitely small distances from each other. The complete circuit can then be treated as two networks, one comprising all the digital devices and the other consisting of the conductor structure. The two networks are connected by $N$ two-terminal ports, as shown in Fig. 1.

To illustrate how these ports are defined, let us consider a 14-pin hex-inverter IC embedded in a digital circuit. Using one pin (i.e., pin 7) as the reference terminal common to all the ports, it is possible to create a maximum of 13 ports on this chip. However, in the generic representation of Fig. 1, each port has its own input and return terminals which carry equal and opposite currents. Therefore, our 14-pin chip must be cast into a 26-terminal device in which the sum of the currents flowing out of the 13 return terminals is equal to the current flowing out of pin 7 on the chip. The use of 13 return terminals in the model to account for the total current flowing into pin 7 is required for compatibility with microwave circuit simulators which use port-defined, rather than node-defined, voltages and currents.

To analyze the field-exposed digital circuit with a simulator, we must first replace the incident RFI field by lumped generators. It has been shown in [11] that the effect of the field on an $N$-port network can be taken into account by augmenting the unexposed network in Fig. 1 with a current source connected across each port, as shown in Fig. 2. The currents generated by these sources are equal to the port currents of the wire structure when it is exposed to the incident field, and all its ports are terminated with short circuits. The solid-state components have no influence on the generator currents because they are treated as having zero dimensions. The passive wire network can simply be represented by a passive black box with its set of network parameters $(Y, Z, S, \cdots)$, where these parameters and the generator currents have to be determined by numerical methods.

Several numerical methods are currently available for EMC applications (see [12]). Although none of these methods is practical for analyzing large scale digital circuits, a subsystem having a few tens of ports, such as a bus cable between two circuits, is manageable. The implementation of the thin-wire method of moments presented in [13], [14] was found accurate for modeling a wide variety of conductor structures, from small loops to long wire antennas. Therefore, this program has been adopted as the modeling tool in this study.

## III. Failure Prediction in Large-Signal Regime

The method proposed in Section II, to represent field-exposed circuits, will now be illustrated with examples. The number of gates in the circuits considered will be kept small to better understand the nature of the failure mechanisms involved. We will assume that interference-free input signals of 0 or 5 volts are applied to the circuit. For a quiescent logic circuit, we can define the failure threshold as the level of incident field that will cause the output voltage(s) to shift above the input-low $(V_{IL})$ or below the input-high $(V_{IH})$ voltage levels for the logic family being used. To reach such offsets at the output of the circuit, the magnitude of the disturbance induced by the RFI has to be large enough to cause the gates to operate in a nonlinear portion of their characteristics. Therefore, small-signal models for the chips are not adequate, and it is necessary to use large-signal analysis to simulate this threshold-crossing failure.

Three difficulties are encountered in carrying out this analysis. First, accurate nonlinear models are not known for most commercially available logic gates, and the extraction of these models is a formidable task (see [4]). Second, the characteristics of the conductor structure (i.e. $Z, Y, S$ parameters) have to be known for a wide frequency range, which may include many harmonics of the RFI field. Furthermore, if a lumped element-based circuit simulator is used to analyze the system including the digital components and the wire structure, a broadband equivalent circuit model has to be derived from the network parameters. Third, the simulation of nonlinear circuits in the time or frequency domain generally requires considerable CPU and memory resources compared to linear circuits with the same number of ports.

For our examples, we have chosen a CMOS inverter (RCA model CD4007A), for which a nonlinear model has been obtained by Liu [4]. This gate has a maximum switching frequency of about 5 MHz. Large signal simulations were performed with LIBRA (EEsof Inc.), which implements a harmonic balance algorithm for the analysis of nonlinear circuits.

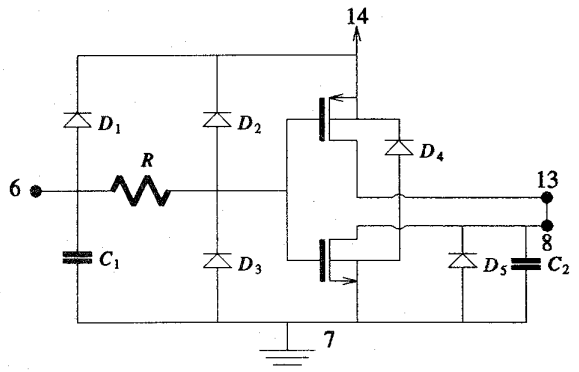



Fig. 3. Simplified circuit diagram of the CMOS inverter on the RCA CD4007A chip. The numbered nodes correspond to the pin numbers on the chip package.

In the harmonic balance solution, the voltage waveforms at all ports are represented by their spectral components, consisting of a dc level, the frequency of the disturbance source, and a finite number of harmonics of this frequency. An iterative procedure is used to find the amplitude and phase of these spectral components that minimize the residual error on the current continuity condition (Kirchhoff's current law) at all the ports.

For all the examples discussed in this paper, the spectrum was truncated to ten frequencies (dc to 45 MHz), which is the maximum allowed by the program, and the $S$-parameters of the structure were evaluated at these frequencies. Since LIBRA is intended for microwave circuit analysis, its library contains JFET models but no MOSFET models. To simulate CMOS gates, MOSFET equivalents were created by adjusting the physical parameters of the JFET models. There are limitations to this approach because some intrinsic second-order effects present in MOSFET's cannot be taken into account accurately in the equivalent JFET's [15]. However, simulations of logic transitions with SPICE showed very small differences between the inverter using the exact MOSFET models and the inverter based on the JFET models. A complete circuit diagram of the inverter is shown in Fig. 3. Components $D_1, D_2, D_3$, and $R$ form the input protection circuit and $D_5$ is the output protection diode. Diode $D_4$ represents the parasitic P-well-to-N-substrate junction. The node numbers on the figure correspond to pin numbers on the chip package.

### A. Square Loop Structure

The first example to be analyzed consists of two inverters connected to each other, with two wires forming a large square loop and subjected to an incident RFI wave, generated by a nearby antenna (see Fig. 4). The size of the loop is similar to the overall dimensions of typical PCB's, and the incident field has been chosen for maximum inductive coupling. The $S$ parameters of the two-port formed by the loop were calculated with the method of moments and passed to LIBRA in a look-up table.

For plane-wave illumination, simulations have shown that the maximum induced voltages at the ports of the loaded square loop occur for a wave propagating along the $x$ axis, with its electric field parallel to the $y$ axis. Fig. 5 shows the voltage waveforms induced at the output of gate A ($V_1$) and at the input of gate B ($V_2$) when the input of gate A is at 0 and 5 volts. The $\hat{y}$-polarized incident electric field has a frequency of 5 MHz and an amplitude of 10 V/m, which is one of the radiated susceptibility levels used in military standards.

The largest disturbance (which in Fig. 5 is the amplitude of the sine wave) occurs at the input of gate B ($V_2$) and has a peak value of about 160 mV superimposed on a 5-V base. A smaller amplitude is observed at the driver end (port 1) because of the low output impedance of gate A. The loading at port 2 is dominated by the parasitic capacitance at the input of gate B. There is not much difference between the high-state and low-state disturbances because of the symmetry present in CMOS inverters. At this level of interference there are no nonlinear effects in evidence, and the disturbance at port 2 is not large enough to induce a change in logic state at the output of the circuit (the switching threshold is 2.5 V).

An extreme radiated susceptibility test specified in MIL-STD-461B uses an incident field of 200 V/m. This condition was simulated and the results are shown in Fig. 6, along with the 50 and 100 V/m cases. The voltage waveforms are given at the input ($V_2$) and output ($V_3$) ports of gate B for a low input condition at gate A. The clipping of voltages larger than 5 V by diode $D_1$ is clearly visible on the $V_2$ waveform. Also, $V_2$ drops below the switching threshold of 2.5 V. However, the time spent by $V_2$ under the threshold is not long enough to induce a change in the logic level at the output of the gate. The 2-V spike at the output gate B ($V_3$ waveform) does not reach the 2.5-V threshold. While it would not cause a wrong logic value, such a pulse can affect the timing of the logic signals in the circuit [16].

In practice good designers would not allow such large loops to be formed on a PCB. Calculations were also done for a more realistic case in which the $y$ dimension of the loop is 1 cm instead of 30 cm. As expected, the level of coupling decreased greatly. For an incident field of 200 V/m, the magnitude of the induced disturbances on $V_1$ and $V_2$ is of the order of 60 mV. In this case, it is clear that nonlinear analysis is not necessary.

### B. Square Loop with Arms

The previous example dealt with a stand-alone square loop. We will now consider a situation that is more commonly encountered. Circuits are normally connected to cables of various lengths, the effect of which can be taken into account in our model by adding long wires to the bottom section of the loop, as shown in Fig. 7. This kind of structure has been used for emission prediction [17], [18] and, by virtue of reciprocity, it should be equally relevant for radiated susceptibility studies.

The largest coupling occurs when the incident field is parallel to the bottom wire and when the frequency is such that this wire forms a resonant dipole. For the example shown here, the wire is half-wavelength long. The coupling mechanism to the loop containing the two inverters is very different than in the previous example where the incident electric field was in the $\hat{y}$ direction. The latter resulted in disturbances at ports 1 and 2 that were nearly in-phase (see Fig. 5), indicating that

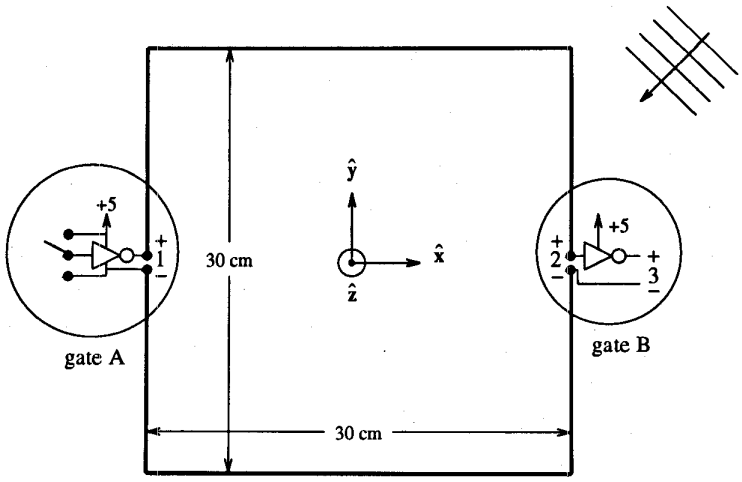



Fig. 4. Wire structure to study RFI-induced static failures in CD4007A inverters. The components within the circles are considered lumped.

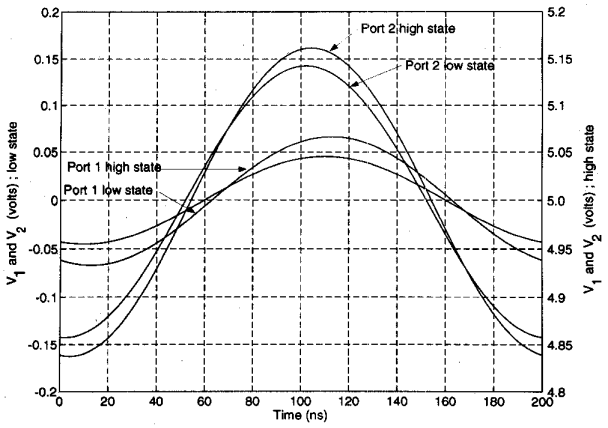



Fig. 5. Steady-state waveforms at ports 1 and 2 over one cycle of 10-V/m 5-MHz RFI.

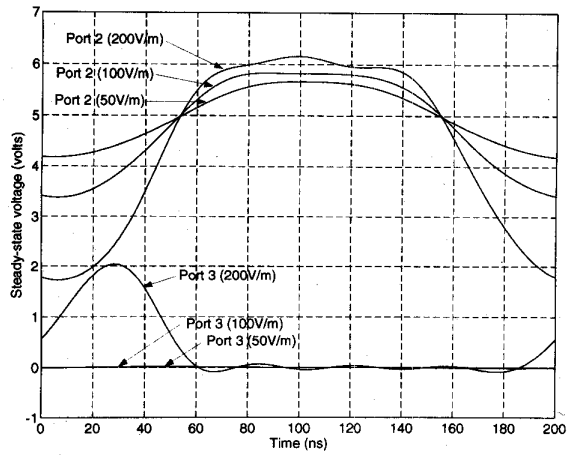



Fig. 6. Steady-state voltage waveforms at port 2 and at port 3 for an interference frequency of 5 MHz and incident fields of 50, 100, and 200 V/m. Port 2 is at a high logic level (5 V) in the absence of interference.

capacitive coupling was dominant. When the arms are present, the loop is exposed not only to the incident field, but also to the field scattered by the long dipole. Close to the dipole, the

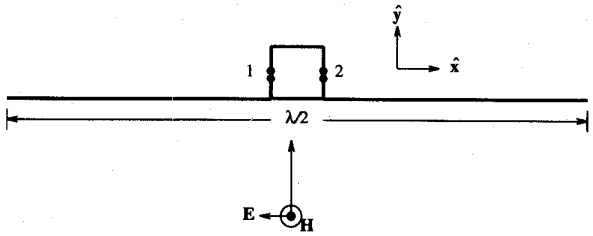



Fig. 7. Wire structure augmented with a resonant dipole to increase EMI coupling.

scattered field can be many orders of magnitude stronger than the incident field. In the case of Fig. 7, a strong magnetic field is generated locally by the dipole current, leading to inductive coupling and to voltage disturbances that are 180° out of phase at ports 1 and 2.

The induced waveforms for a 5 MHz incident field of 2 V/m are shown in Fig. 8. The input of gate A was set to logic low (0 V) for this simulation, as was the case in Fig. 6. Without interference, $V_1$ and $V_2$ are both high (not shown). But as the figure shows, interference forces ports 1 and 2 to be in different logic states for most of the 200 ns cycle, in spite of the short separation between these two ports ($\lambda/100$) at the RFI frequency. This difference is indicative of a predominant inductive coupling in the loop. The clipping of the applied sinusoidal disturbance above the 5-V level is clearly visible at ports 1 and 2. At port 1, this is due to the PN junction formed by the drain of the PMOS and the $N$ substrate in gate A. At port 2, the clipping is done by diode $D_1$ in gate B.

Fig. 8(a) shows that the amplitude of the interference is sufficient to cause $V_3$, the output of gate B, to switch to the high state, with the potential of causing failures in a logic system. Comparison with Fig. 6 shows that the presence of the arms has increased the susceptibility level by a factor of more than 100 (40 dB). While Fig. 6 shows no failure ($V_3$ does not cross the switching threshold of 2.5 V) for an incident field of up to 200 V/m, Fig. 8(a) shows that a field of 2 V/m is sufficient to cause failure.

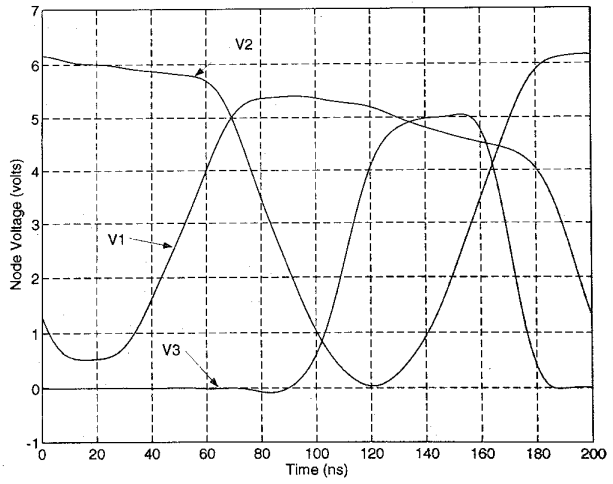



Fig. 8. (a) Waveforms at ports 1, 2, and the output of gate B ($V_3$), obtained with the method of harmonic balance for the geometry shown in Fig. 7. The RFI field has an amplitude of 2 V/m peak and a frequency of 5 MHz. The normal low and high logic levels are 0 and 5 V. (b) Same as Fig. 8(a), but for loop dimensions of 1 cm × 30 cm and $|E_{\text{inc}}| = 30$ V/m.

The calculations were also done for the case where the $y$ dimension of the loop is 1 cm. Results are shown in Fig. 8(b) for an incident field amplitude of a 30 V/m. Without disturbance, node 3 is at 0 V. The results show that interference has induced a 50-ns wide logic-high pulse on the $V_3$ waveform. Rapid oscillations can be seen on the low logic level of $V_3$. The frequency of these oscillations corresponds to the ninth harmonic of the incident signal, which was the highest frequency considered in the harmonic balance analysis.

## IV. Failures in Small-Signal Regime

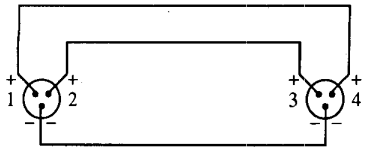
The failures described in the previous section are caused by interference signals whose amplitude is comparable to the distance between logic levels. They occur even if the victim digital circuit is in a quiescent state. For this reason, they have been called static failures. For fast-switching circuits, it is not necessary to induce such a strong disturbance to cause failure. A change in the timing of a logic transition, which can be induced by much lower levels of interference, can lead to malfunction [5]. It has been demonstrated in [7] that the amount by which a logic transition is delayed by RFI is directly related to the amplitude of the RFI disturbance present on the quiescent logic signal before the transition is initiated. Thus, it is not necessary to simulate the actual logic transition to predict the amount of delay induced by interference. In the case of RFI, it is sufficient to simulate the circuit in steady state, as we did in Section III. Furthermore, since the disturbances leading to timing failures are much smaller that those required for static failures, a linearized, small-signal model can be used for the digital circuit, thus reducing the computing and modeling efforts considerably.

In order to analyze a semiconductor circuit in the small-signal regime, a nonlinear analysis must first be performed to establish the dc bias point and determine the small signal parameters of the semiconductor devices. These parameters are then used in the ac analysis together with the models of the wire structure and the current sources replacing the incident field (see Fig. 2). Since the ac analysis assumes a linear behavior of the circuit, it is not necessary to use the harmonic balance program. SPICE is a convenient tool that is widely used for the ac and dc simulation of integrated circuits. However, except for some commercial versions, SPICE can only deal with circuits composed of lumped elements selected from the program's library (inductor, capacitor, resistor, ...). Hence, the $N$-port network derived in Section II must be represented by an equivalent network of lumped elements that is valid at the RFI frequency of interest. The network must also be valid at dc to calculate the bias point.

There is a significant difference between the LIBRA and SPICE models of the wire structure in the treatment of ground terminals. Microwave circuit simulators like LIBRA use port-defined voltages (and currents), that is, voltages defined between the "+" and "−" terminals of each port. This definition is convenient for distributed circuits like the wire structures of interest here. Lumped circuit simulators like SPICE use node-defined voltages, that is, the voltage between individual nodes and a common reference terminal. For instance, in the example four-port network of Fig. 9(a), ports 1 and 3 on the wire structure have their "−" terminals at different locations, and these terminals can therefore be at different ac voltages. In Fig. 9(b), the equivalent $\pi$ network model to be used in SPICE has a single "−" terminal for all the ports, identified with the ground symbol. This means that an arbitrary $N$-port wire structure, which has $2N$ terminals, will need to be represented by a $\pi$ network having $N+1$ terminals. To have the same ac node voltages and currents in the two cases, the same port excitation must be present. This is readily accomplished by placing the current sources in Fig. 2 across the ports of the $\pi$ network.

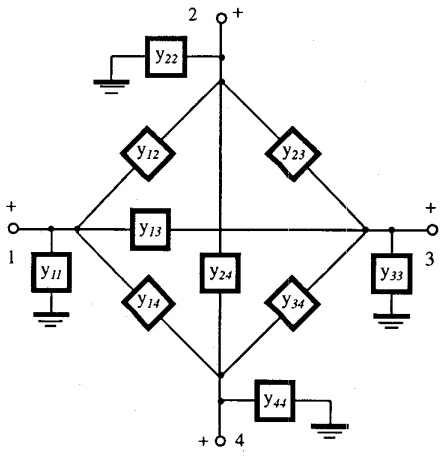
The required $N$-port $\pi$ network can be generated as illustrated by the example in Fig. 9. Each element in the $\pi$ network has an admittance $(y_{ij})$ that is related to the admittance parameters of the original $N$-port wire structure $(Y_{ij}^{ws})$ by [11]

$$y_{ij} = -Y_{ij}^{ws} \tag{1}$$




Passive 4-wire network

(a)




Equivalent $\pi$ network

(b)

Fig. 9. Circuit representation for a four-port wire network. (a) Passive four-wire network; (b) equivalent $\pi$ network. The terminals labeled "−" are the reference terminals for the port voltages.

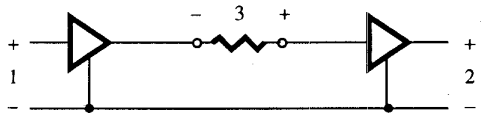



Fig. 10. A three-port network with a floating component.

when $i \neq j$, and

$$y_{ii} = \sum_{k=1}^{N} Y_{ik}^{ws}. \tag{2}$$

Since dc analysis has to be performed when nonlinear components are present, (1) and (2) have to be valid at ac and dc. In other words, the dc connections present in the original wire structure between the various ports have to be the same as in the $\pi$ network.

An equivalent $\pi$ network can be derived as described above, provided that the dc resistance of the wires is negligible and the ports of the original network can be chosen to have a common reference terminal at dc. That is, this approach cannot be used in the presence of "floating components" such as the resistor in Fig. 10. There is no terminal that is common to all three ports of this network at dc. The circuit can be handled only if the resistor is physically close to the device at either end of the connection, in which case it can be incorporated in the model for that device.

Once the $y_{ij}$ values are calculated, lumped elements having the same ac and dc admittance can be derived and inserted

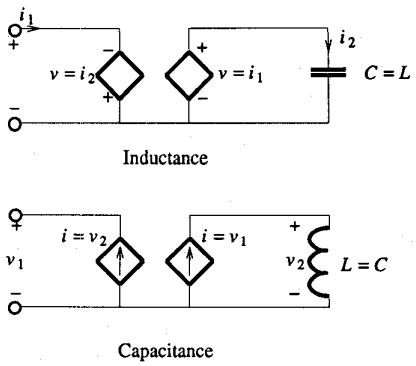



Fig. 11. Implementation of negative inductance and negative capacitance using active-circuit equivalents.

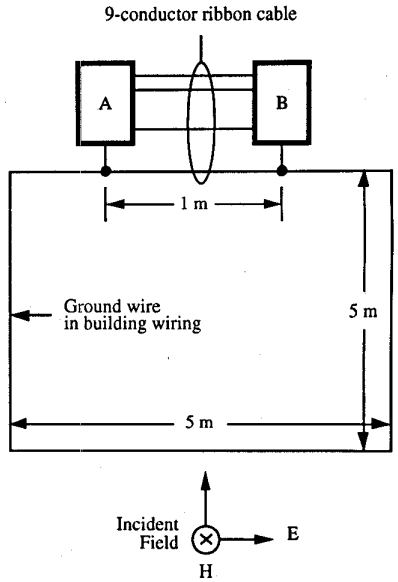



Fig. 12. An example circuit with a ground loop.

in the corresponding branches in the $\pi$ network. For zero dc impedance branches, the equivalent circuit consists of an inductor in parallel with a resistor. Zero dc admittance branches are implemented by a capacitor in series with a resistor. In each case, the $R$ and $L$, or $R$ and $C$, values are selected to satisfy (1) and (2) at the ac frequency of interest. In some cases, this computation may lead to negative $R, L$, or $C$ values. Since some early versions of SPICE (e.g. version 2G6 from Berkeley) do not support negative capacitance or inductance, such components may be generated with controlled sources as shown in Fig. 11.

As an example for the small-signal approach, consider the circuit shown in Fig. 12. Device A drives device B with eight independent signals over a 1-m long ribbon cable. Assuming that the two devices use different power outlets and that no RFI filters are used between the signal ground and the power cord of the device, a large, low-impedance loop may be formed by the external wiring, as shown. The currents induced in this loop by radiated interference may cause significant disturbances on the signals propagating on the ribbon cable.

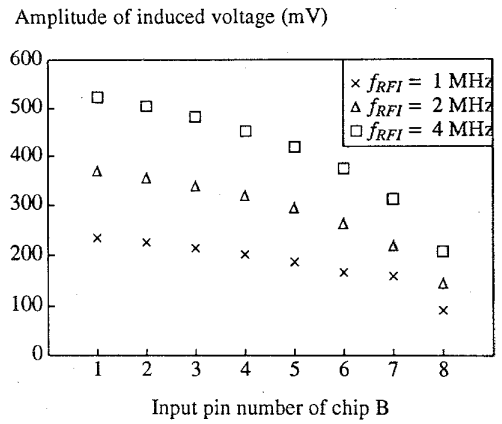



Fig. 13. Voltages induced at the input pins of the circuit in Fig. 11 by a 10 V/m incident plane wave.

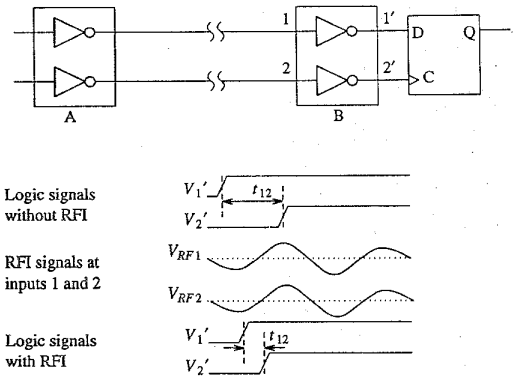



Fig. 14. RFI-induced change in the time interval $t_{12}$ between signals $1'$ and $2'$ at the output of circuit B.

For this simulation, all the wires are 1 mm in diameter and the center-to-center wire spacing in the nine-wire ribbon is 2 mm. The effect of wire insulation was neglected. The sixteen-port network was analyzed with the thin-wire MoM program, and an equivalent lumped-element model was derived for each frequency of interest. A utility program was written to convert automatically the field analysis results into SPICE input lines. Sixteen CMOS inverters, eight at each end of the line, served as drivers and receivers, and Liu's model for the RCA CD4007A [4] was used in the simulations. It should be mentioned that since the analysis is done in the linear regime, there is no need for such a sophisticated nonlinear model. A small signal model obtained from measurements could be used.

A 10 V/m incident plane wave linearly polarized as shown in Fig. 12 was applied to the structure at frequencies of 1, 2, and 4 MHz, which are smaller than the fastest switching frequency of the inverters (5 MHz). The amplitude of the induced disturbances at the input ports of device B as predicted by SPICE is given in Fig. 13. The figure shows that the interference amplitude increases with increasing distance between the logic signal line and the reference line. For this simulation, a low logic state was applied to the cable by the drivers.

The interference signals perturb the timing of logic transitions at the output of the inverters in device B. For the cable in Fig. 12, the RFI-induced delay can be calculated from the steady-state disturbances given in Fig. 13, as explained in [7]. Since the induced delay depends on the phase of the RFI signal at the time of the transition, the change in propagation delay will not necessarily be the same for all eight signals. For the case shown in Fig. 14, signal 1 experiences a positive delay, while the delay on signal 2 is negative. This results in a skew between these two lines, given by

$$\text{skew} = \max(|t_{12} \text{ with RFI} - t_{12} \text{ without RFI}|) \qquad (3)$$

where $t_{12}$ is the interval defined in the figure. This skew could cause failure if $t_{12}$ is critical to the operation of device B. In the case of Fig. 14, a failure is likely to occur if $t_{12}$ becomes smaller than the setup time of the flip-flop. Such failures have been demonstrated experimentally [6]. The maximum delay values for line 1 and the minimum delay values for line 2, which are the two most perturbed lines on the cable, can be calculated from the results in Fig. 13, and they are given in Table I. The table shows that the worst case skew can be as high as 60 ns at an RFI frequency of 4 MHz. It should be mentioned, however, that the calculated delays depend greatly on the characteristics of the gates, particularly on the rise and fall times of the logic transitions. Since the occurrence of a failure is dependent on the timing of the switching logic signals, it has been called dynamic failure.

TABLE I
DELAYS IN THE CIRCUIT OF FIG. 11

| f (MHz) | max $\Delta t_1$ (ns) | min $\Delta t_2$ (ns) | skew (ns) |
|---|---|---|---|
| 1 | 15.7 | -11.7 | 27.4 |
| 2 | 26.4 | -18.3 | 44.7 |
| 4 | 33.8 | -26.2 | 60.0 |

## V. CONCLUSION

Two methods have been developed to investigate the effects of radiated RFI on the operation of logic circuits, one for large signals and one for small signals. Both methods are based on the utilization of circuit simulators that allow accurate modeling of the solid-state devices forming the logic circuit. In the circuit simulator environment, incident RFI fields are replaced with an equivalent set of current sources, and the circuit wiring is replaced with an equivalent network. The source currents and the admittance parameters of the wire structure are derived using a thin-wire moment-method code.

Large-signal analysis can be used to predict the likelihood of static failures, which occur when the interference causes the quiescent logic state of a circuit to change into the complementary state. The magnitude of the induced RFI is strongly dependent on the geometry of the wires forming the circuit. For instance, a wire structure similar in size to typical dimensions of printed circuit boards did not cause static failures in a CMOS circuit, even for an incident field of 200 V/m. On the other hand, static failures were observed for an incident field of only 2 V/m when the structure was augmented with a parasitic resonant dipole resulting from building wiring. The simulation

tool used for large signal analysis uses a harmonic balance algorithm to predict the steady-state response in the nonlinear regime. This approach requires extensive computing resources, and hence its applicability is limited to the investigation of circuits having only a few gates.

In the linear small-signal regime, it is possible to handle a larger number of gates. Although this approach cannot be used to predict static failures, it can be used to predict dynamic failures. The RFI signal induced in the circuit while the logic states are in their quiescent state can be used to predict the perturbation in the timing of logic transitions, which is the main cause of failure in this case. The ability to predict these failures for a given incident field should be of considerable utility to the circuit designer. The disturbance amplitude may be calculated using a circuit simulator to analyze a network model of the wire structure connected to the solid-state devices. In the case of SPICE, a lumped-element model is needed. A method to derive such a model in the form of an $N$-port $\pi$ network has been presented. This network has to be valid at dc, to allow nonlinear analysis to be used to establish the dc operating point of the circuit.

Unlike multiconductor transmission line models which are broadband but have inflexible geometry, the approach taken in this paper can handle the arbitrary wire geometries found on real circuit boards.

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