Fast-Transient Susceptibility of a D-Type Flip-Flop

R. E. Wallace, S. G. Zaky, and K. G. Balmain

Abstract—**Human electrostatic discharge (ESD) produces a transient current pulse with a very fast risetime, which can be a source of electromagnetic interference in digital devices. The focus of this paper is the radiated susceptibility of D-type flip-flops implemented in various CMOS and TTL logic technologies. A transient impulse was used to simulate the radiated field produced during an ESD event. A synchronized-disturbance testing methodology is developed that allows accurate control of the instant at which the disturbing signal is applied to the data input lines during an operational cycle of the circuit. The study reveals that these devices are susceptible only during certain time intervals during an operational cycle. The particular interval during which a flip-flop is susceptible is dependent on the logic state of the data input line, the implementation technology of the flip-flop, and the amplitude of the disturbing signal. The total width of the susceptibility intervals is a device parameter that can be used to determine the probability that the flip-flop will fail in the presence of random transient interference pulses.**

I. Introduction

For many years, research has been conducted on the effect on electronic systems of various fast-transient disturbances such as nuclear electromagnetic pulse (NEMP), lightning, and electrostatic discharge (ESD). Of these, ESD events occur most frequently, and their effect on digital equipment has become a major concern in the electronics industry.

It has been reported by Wilson *et al.* [1] that the electric field strength generated by an ESD arc can be greater than 150 V/m within 1.5 m of the discharge, and there is significant radiation from the body of a typical discharge simulator. A device in the vicinity of an ESD event may fail as a result of being subjected to radiated EMI in the indirect discharge case, or to a combination of radiated and conducted EMI in the direct discharge case. For a complete understanding of the failure mechanisms, it is essential to investigate the susceptibility of the device to the radiated fields produced by an ESD event.

In standard test procedures, the susceptibility of a device under test (DUT) to an ESD event is evaluated by subjecting given test areas on the DUT to the EMI generated by the discharge current impulse. It has been stated by several researchers that the susceptibility level of a digital circuit depends on the operational state of the circuit at the time the disturbance is applied (see, for example, Rhoades [2], Calcavecchio and Pratt [3], and Nick *et al.* [4]). Existing testing procedures require that multiple tests be performed per test area to increase the probability that one of the ESD events will coincide with the most susceptible operational state [2]–[5]. According to Staggs and Pratt [5], the number of tests performed by many manufacturers is 50 tests per test area; however, some advocate the use of 10 000 or more tests per test area [3], [4]. The result of such experiments is a probability of failure within a given confidence interval.

The focus of the work presented here is the issue of how to characterize the radiated transient susceptibility of a single D-type flip-flop, implemented in various logic technologies. Existing radiated susceptibility test methods utilize plane wave disturbance coupling techniques [4], which result in the entire DUT being subjected to the interfering field. Thus, when failure occurs, it is difficult to identify its cause. In order to gain a more detailed understanding of the failure modes induced by transients, experiments were conducted in which the interfering signal was coupled exclusively to one circuit node, namely, the data input of the flip-flop. Furthermore, the instant at which the disturbance was applied relative to the operational cycle of the flip-flop was controlled. This control enabled a sequence of synchronized disturbance tests to be conducted on a variety of CMOS and TTL flip-flops, and the test results are reported below. We begin by describing the test setup used.

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TABLE I
FLIP-FLOPS TESTED, WITH THEIR MAXIMUM PROPAGATION DELAY AND MAXIMUM CLOCK FREQUENCY AS SPECIFIED BY THE MANUFACTURER

Implementation	Designation	Maximum Propagation Delay (ns)	Maximum Clock Frequency (MHz)
Low-power Shottky TTL	74LS74	19.0	25
High-speed CMOS	74HC74	17.5	25
Standard TTL	7474	17.0	25
Advanced Low-power Shottky TTL	74ALS74	11.5	34
Advanced Shottky TTL	74AS74	6.25	105
Shottky TTL	74S74	6.0	110
FAST TTL	74F74	5.75	100
Advanced CMOS	74AC74	5.5	140
Advanced CMOS (TTL compatible)	74ACT74	5.5	145

II. Test Setup and Methodology

In this section, a test setup and methodology are developed to investigate the susceptibility of a single D flip-flop to an ESD pulse. The device chosen for testing is the commonly used D flip-flop having the generic designation number "7474" (e.g., 74LS74 identifies the low-power Schottky implementation of this particular device). The 7474 flip-flop is a positive-edge-triggered device. That is, when the rising edge of a pulse is sensed at the clock input (CLK), the logic value present on the data input line (D) is stored in the flip-flop and appears on the data output (Q) after a short delay. The state (stored value) of the flip-flop does not change until a different logic signal appears at the D input and another CLK pulse is applied. The 7474 flip-flop is available in all of the commonly used TTL and CMOS logic technologies. The implementations that have been tested in this study are summarized in Table I.

A. Test Mount

All the implementations studied are pin-compatible, thereby necessitating the construction of only one test mount. The test mount used in this study, which is shown in Fig. 1, consists of a three-layer board having a signal-trace plane, a ground plane, and a power plane. The flip-flop under test is placed in the chip socket at the center of the board, and the wiring on the board provides access to the D, Q, CLK, and preset (PRE) pins of the flip-flop. Four inverter chips (identification number: 7404) of the same technology as the flip-flop under test are used to drive the flip-flop inputs and to provide a realistic load at the Q output.

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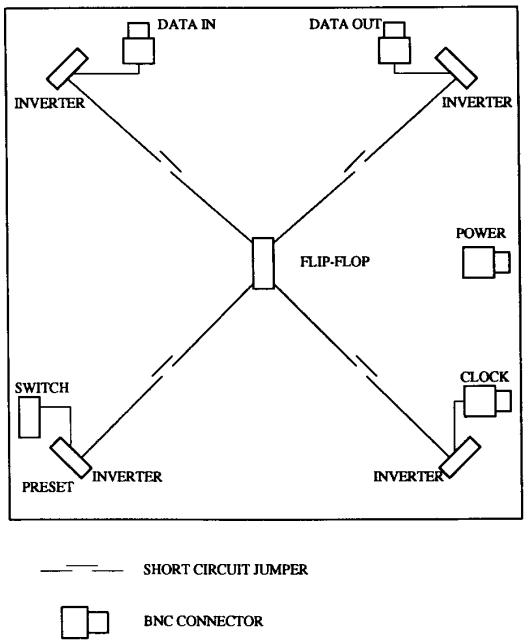

Fig. 1. Top view of the circuit board used for flip-flop testing.

The inverters are connected to external test circuitry via BNC connectors. The traces between the flip-flop and the inverters are microstrip transmission lines of characteristic impedance close to 100 Ω. The four traces are arranged to minimize crosstalk among them and are short enough that reflections do not distort the shape of the induced voltage waveform. Any of the four signal paths may be broken by removing a short-circuit jumper located at the middle of the trace.

B. Disturbance Coupling

The disturbing signal is coupled to a trace by removing the jumper and attaching a square wire loop (3.4×3.4 cm) that acts as a receiving antenna for the radiated disturbing signal. The antenna that transmits the disturbing signal consists of a square loop of the same size with a feed port and a current-monitoring port, which allows the exact shape and amplitude of the current flowing in the loop to be observed. The two loop antennas are placed approximately 1 cm apart and are oriented for maximum coupling.

The polarity of the induced voltage can be controlled by the manner in which the receiving loop is connected to the jumper posts. The coupling loop configuration and its equivalent circuit for producing what will be referred to as a "positive" induced voltage are shown in Fig. 2. The term "positive" is chosen because the above coupling arrangement causes a primarily positive voltage spike to be superimposed on the voltage normally present on the flip-flop pin. Reversal of the receiving loop connections induces a "negative" voltage.

The current pulse fed to the transmitting loop resembles the discharge current waveform produced during a human ESD event. The pulse is obtained using a waveshaping circuit to introduce a "droop" on the flat top of a pulse produced by a fast-risetime, high-amplitude flat-topped pulse generator. The loop current waveshape, as measured at the current monitoring port of the transmitting loop, is shown in Fig. 3. The pulse is approximately 60 ns in duration and has a risetime of 0.9 ns. The peak loop current amplitude is continuously variable from 0 to 3.78 A.

A representative digitized oscilloscope trace of the voltage induced at a signal pin of the flip-flop package is shown in Fig. 4. The waveform is similar in shape to that generated by the ESD simulator used by Wilson *et al.* [1], except that the voltage waveform of Fig. 4 is twice as wide as that presented in the reference. In this regard, it should be noted that the results presented in [1] were generated using a wideband receiving antenna, whereas the results of Fig. 4 were measured through a coupling path of much lower bandwidth (i.e., the receiving loop, the microstrip trace, and the IC's).

The susceptibility results below are given as a function of peak current in the transmitting loop antenna rather than peak voltage induced at the flip-flop signal pin. The transmitting loop current amplitude relates more directly to the incident radiated field strength, which is the parameter of concern in radiated susceptibility testing. For a given loop current, the amplitude of the induced voltage is dependent on the input impedance of the flip-flop and the output impedance of the inverter, and hence on the implementation technology. For example, a peak loop current of 3.78 A leads to a 12 V peak induced voltage for the ACT flip-flop/inverter combination, and to 32 V for the S flip-flop/inverter combination. Hence, loop current is a more meaningful parameter for the purposes of comparing the radiated susceptibility of different types of flip-flops.

C. Methodology

In this work, a circuit or subcircuit is considered to be "static" when it is in a quiescent mode of operation. That is, a circuit is static during the period of time between input signal transitions, provided that this period is much greater than the propagation delay of the circuit. We will use the term "static failure modes" to refer to those errors that occur when a device is not undergoing a change in state as part of its normal operation. A circuit is considered to be "dynamic" when it or one of its inputs is undergoing a change in state. Hence, dynamic failure modes are responsible for those errors that occur while a device is undergoing a change in state as part of its normal operation. The susceptibility study presented in this paper concerns the excitation of dynamic failure modes resulting from corruption of the D line at or about the time a clock pulse is applied to the flip-flop.

Fig. 5 shows a circuit diagram of the test circuit and the predisturbance logic levels at the inputs and outputs of various components. The flip-flop is preset to a high logic level, and a low logic level is applied to the D line. Thus, in the absence of any disturbance, application of a clock pulse should cause the flip-flop to change state from high to low. The disturbance coupling is configured in the "positive" sense, so as to drive the D line high.

A 50-ns clock pulse is applied to the CLK input and the disturbing signal is applied to the D line at a specific time t_d relative to the positive edge of the clock pulse (see Fig. 6). Positive values of t_d indicate the disturbing signal was applied after the positive clock edge; negative values indicate the disturbing signal was applied before the positive clock edge. The state of the flip-flop is sampled about 2 ms after the positive edge of the clock pulse. If the postdisturbance state of the flip-flop is the same as its initial state, then a failure has occurred. A complete test cycle consists of varying the delay time such that the disturbance is swept from 50 ns before the clock edge to 50 ns after in 0.5 ns increments (i.e., $-50\text{ ns} \leq t_d \leq 50\text{ ns}$). Upon completion of one sweep, the disturbance amplitude is increased and the test cycle repeated. The time required to perform one single test in a given interval is 1 s.

The experiment was automated through the use of a personal computer and the circuitry shown in Fig. 7 to generate and synchronize the clock and disturbance signals and monitor the results. The

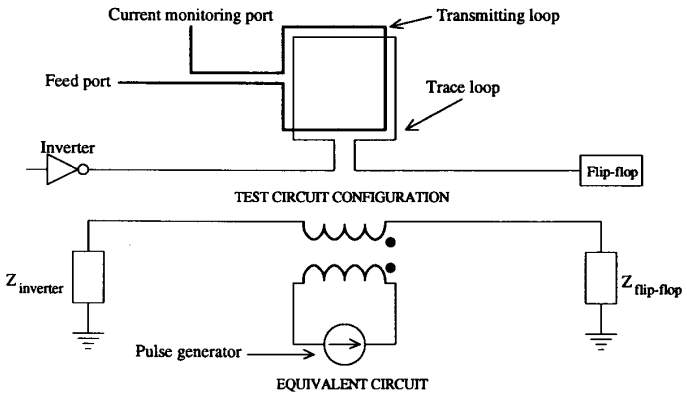

Fig. 2. Test circuit configuration and equivalent circuit for "positive" induced voltage.

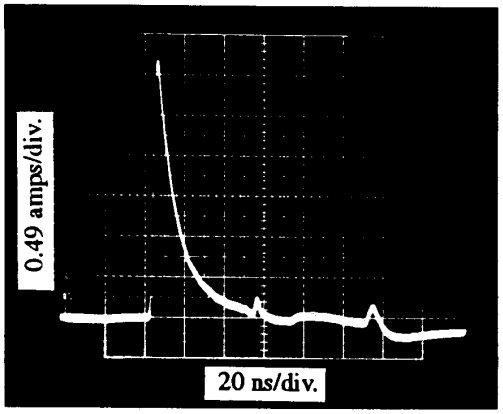

Fig. 3. A typical loop current waveshape as measured at the loop antenna current monitoring port.

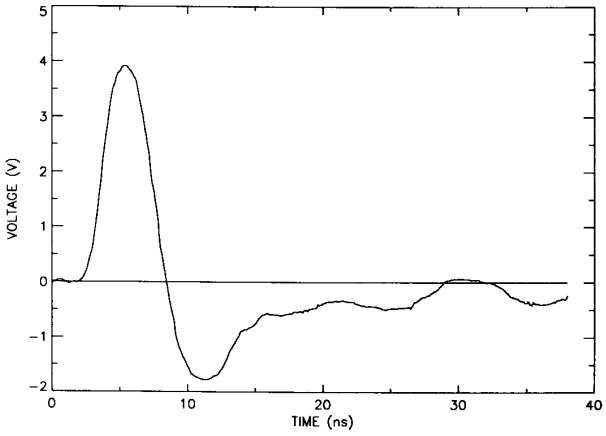

Fig. 4. A representative plot of the induced voltage waveshape as measured at the flip-flop pin for positive coupling.

D/A-A/D card is used by the PC to set the D value, reset the flip-flop, control the amplitude of the disturbance pulse, and measure the postdisturbance Q line voltage. The delaying pulse generator is capable of producing two separate pulses, with a relative delay of 0–1000 s and a maximum delay resolution of 5 ps. It is used to generate the flip-flop clock signal and a triggering pulse for the disturbance-impulse generator.

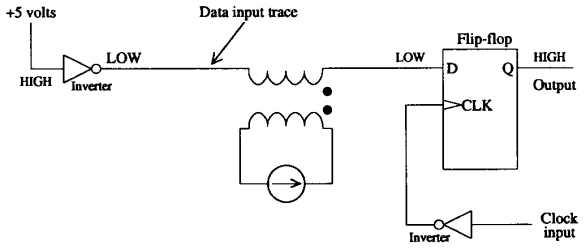

Fig. 5. Pretest circuit conditions when the D line is set to a low logic level.

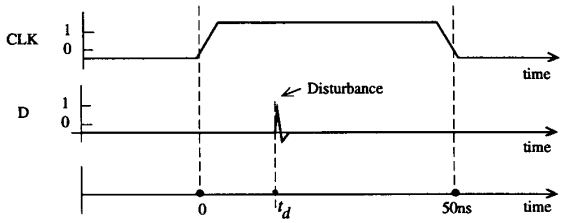

Fig. 6. Disturbance timing. *Notes*: 1) All time intervals measured between waveform 10% amplitude values; 2) negative values of t_d indicate the disturbance occurred before the rising edge of the clock signal.

III. Test Results and Discussion

Fig. 8 shows the results of a test on the 74AC74 chip when configured as shown in Fig. 5. The horizontal axis gives the delay time t_d in nanoseconds, and the vertical axis shows the peak loop current amplitude. Raised portions of the graph represent synchronization times at which failure occurred. There are several distinct ranges of the delay parameter t_d during which failure occurs, which we will call *failure windows*.

The test results obtained for the rest of the CMOS chips [6] are very similar to those shown in Fig. 8. Results for the 74S74, 7474, and 74ALS74 TTL chips are shown in Figs. 9, 10, and 11, respectively. Upon examination of these figures, one can see that the TTL results are different from one another and from the CMOS results. Each chip test reveals a unique failure window position, width, and dependence on loop current amplitude. For example, the failure windows of the 74S74 chip are wider and more numerous than those of the 74AC74 chip.

The width of a failure window is dependent on the amplitude of the disturbing signal. For example, the main failure window in the results for the 74AC74 and 7474 chips (Figs. 8 and 10) is narrowest

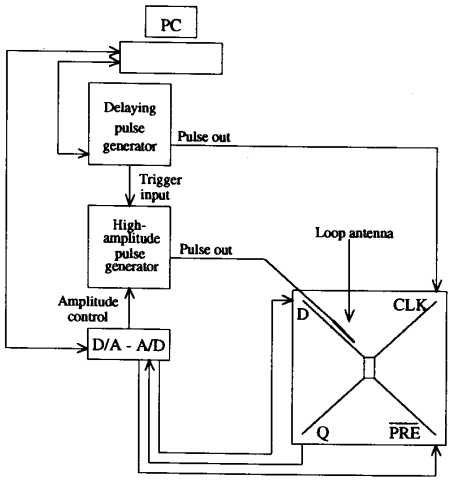

Fig. 7. Block diagram of the experimental setup.

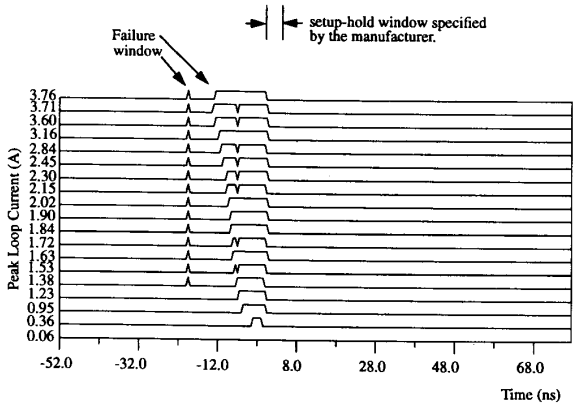

Fig. 8. Dynamic susceptibility results for the 74AC74 CMOS flip-flop. Initial conditions: Q = H, D = L.

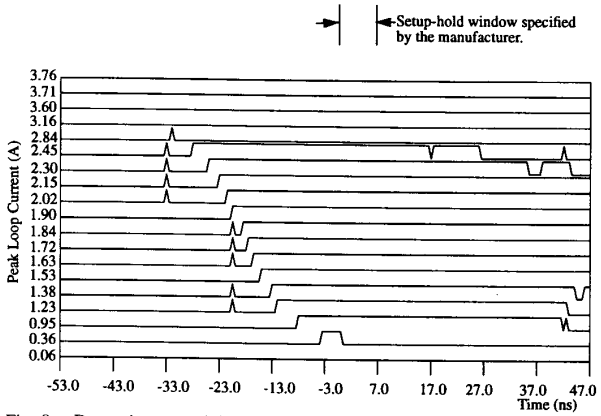

Fig. 9. Dynamic susceptibility results for the 74S74 TTL flip-flop.

at the lowest amplitude and increases in width with disturbance amplitude. The main failure window in the 74ALS74 results (Fig. 11) is narrowest at the intermediate current levels. Examination of the 74S74 results (Fig. 9) reveals that the chip appears to stop failing as the current amplitude exceeds 2.84 A. In fact, the chip does change

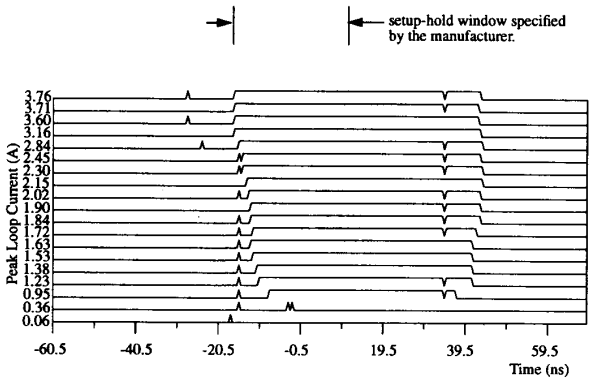

Fig. 10. Dynamic susceptibility results for the 7474 TTL flip-flop.

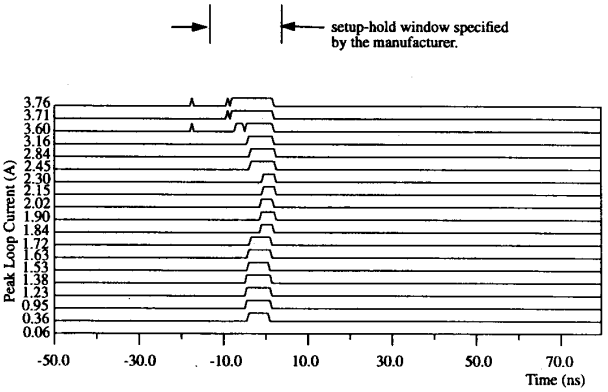

Fig. 11. Dynamic susceptibility results for the 74ALS74 TTL flip-flop.

state above 2.84 A, but does not stay in the new state permanently. Hence, no failure was recorded by the test equipment. A more detailed discussion of this phenomenon is given later in this section.

The position and width of the setup-hold time windows W_{sh}, as specified by the manufacturer for each chip, is shown in the figures. Any fluctuations in the data input signal outside this window, and within the specified operating voltages, are not supposed to affect the operation of the device. Referring to each of the figures, one can see that for low disturbance amplitudes, the failure windows are within the setup-hold window. However, for larger amplitudes, some failures occur outside the setup-hold window. All the tested chips were susceptible to high-amplitude disturbance at certain points outside the setup-hold window. The mechanisms leading to these failures are not yet fully understood.

The above experiments were repeated with the D line at a high logic level, a negative disturbance, and the flip-flop in the 0 initial state. For the CMOS chips, the results of these tests are almost identical to those given in Fig. 8 for the D-line-low tests. The reason for this is thought to lie in the fact that the input and output stages of CMOS gates are almost symmetrical with respect to power and ground. This gives the chip state-independent susceptibility to transients, in addition to static noise margins, risetime, falltime, and propagation delay.

The TTL results for the D-line-high tests are markedly different from those obtained for the D-line-low rests. As an example, the test results for the 74ALS74 chip are shown in Fig. 12. One can see that these results are by means similar to those shown in Fig. 11 (the D-line-low test results). The failure window in Fig. 12 begins at a higher current amplitude and shows a completely different variation with amplitude than the failure window in Fig. 11.

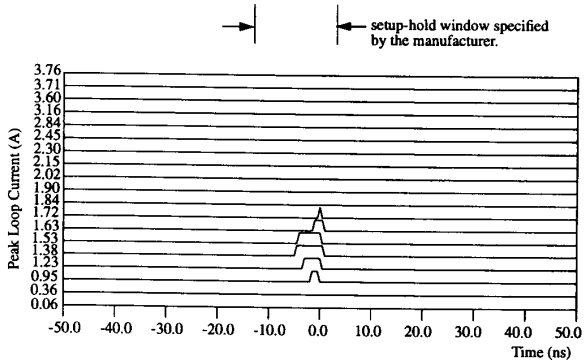

Fig. 12. Dynamic susceptibility results for the 74ALS74 TTL flip-flop. Initial conditions: Q = L, D = H.

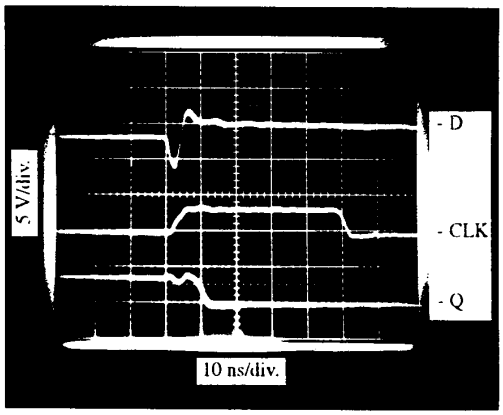

Fig. 13. Signals at D, CLK, and Q for a peak disturbance. Loop current of 0.56 A and initial conditions Q = D = H. A failure is recorded because Q changes to low and remains low.

All of the TTL chips, with the exception of the AS and F chips, show no failures for loop currents in excess of a certain value in the case of D-line-high. This can be explained by examining the switching process in detail. Fig. 13 shows the effect on the 74S74 chip of a 0.56 A loop current impulse (a relatively low loop current amplitude). The top oscilloscope trace shows the D line which is in the high logic state. The disturbance pulse, which occurs inside the setup-hold window, causes the voltage on the D line to drop from 3.4 V to −1 V, then rise to 7 V. The D-line voltage decays back to 3.4 V after 40 μs. The middle oscilloscope trace shows the CLK signal. The lower oscilloscope trace shows the Q signal, which is initially at a high logic level. Correct operation in this case requires that Q remain high. However, because of the disturbance, Q switches from high to low; and since it remains in the low state, it is recorded as a failure.

The results for a loop current of 1.75 A are shown in Fig. 14. The disturbance pulse drives the D line to −5 V before the protection diode switches on and limits the voltage to about −0.7 V. During the positive pulse, the voltage on the D line rises to +10 V before it is clipped. In this case, the Q line switches from high to low, as expected, but then switches back to a high logic value. The overall effect is a nonpermanent switching of the flip-flop, which is recorded by the test equipment as "no failure." This is the reason that some of the failure windows shown earlier become narrower, and may ultimately cease to exist, as the disturbance current is increased.

Regardless of whether one is interested in permanent or temporary failures, the susceptibility of all the TTL chips tested is state

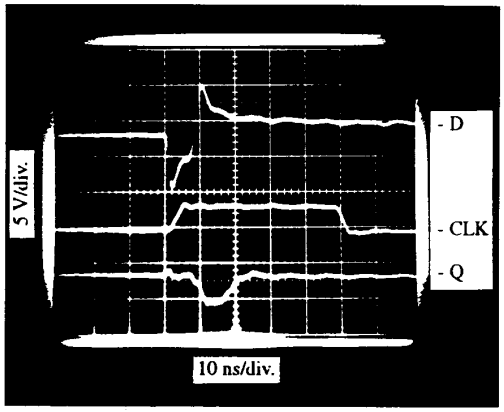

Fig. 14. Signals at D, CLK, and Q for a peak disturbance. Loop current of 1.75 A and initial conditions Q = D = H. No failure is recorded because Q switches to low then returns to high.

dependent. TTL devices are not symmetrically constructed; therefore, symmetric operation is not expected.

Among those tested, the least susceptible chip is the 74LS74. A peak loop current of 0.95 A or more is needed to induce failure, and this failure occurs only when the D line is in the high state. The next least susceptible chip is the 74HC74, requiring 0.95 A to induce failure for both D line states. The most susceptible chips are the 74AC74, 74ACT74, and 74F74, all failing for either D line state at a peak loop current of 0.36 A. Referring to Table I, one can see that the least susceptible chips are the slowest, or lowest bandwidth chips, whereas the fastest (highest bandwidth) chips are the most susceptible. Thus, bandwidth plays an important role in determining the level of external field that can be tolerated before an upset occurs.

The results reported in Figs. 9–12 are highly repeatable. The positions of the failure windows did not vary by more than 0.5 ns between tests (on the same IC), and the widths of the failure windows were consistent to within 1 ns. These are the limits imposed by the 0.5 ns step size used.

IV. Random Disturbance: The Probability of Failure

The tests reported in this paper used a disturbing pulse that is synchronized relative to the clock edge. In practice, a disturbance will occur at random when caused by an external event such as ESD. In this case, the probability of failure is the probability that a disturbance will occur inside one of the failure windows of the device, as defined above. Let W_f be the sum of the widths of the failure windows at a given disturbance amplitude. The probability of failure is a function of W_f and the clock period. For example, for the 7474 flip-flop (D line low) at a disturbance amplitude of 1.23 A, $W_f = 52$ ns. If this flip-flop is driven by a 10 MHz clock, i.e., a clock period of 100 ns, the probability that a given disturbance will fall within the failure window is given by

$$P(\text{error}) = \frac{W_f}{\text{clock period}} = \frac{52}{100} = 0.52.$$

As another example, consider the 74AS74 and 74S74 flip-flops. Although they have similar operating speeds, dynamic susceptibility tests reveal that the failure windows (permanent failures only) for the 74S74 were not only more numerous than those of the 74AS74 but wider as well. If it is assumed that during normal operation in a circuit the D line has an equal probability of being high or low, then the probability of failure is calculated using the average W_f for both states. The failure probabilities for both flip-flops are shown in

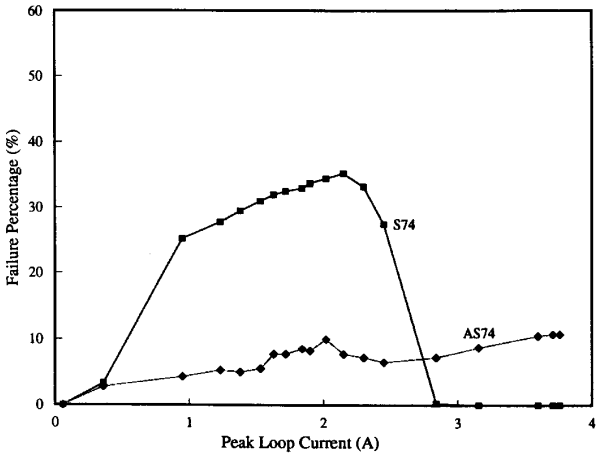

Fig. 15. Probability of failure of the "S74" and "AS74" flip-flops operating at a clock frequency of 10 MHz, averaged for different initial conditions.

Fig. 15, for a clock frequency of 10 MHz. For a randomly occurring disturbance, the 74S74 chip is much more likely to fail.

In conclusion, W_f is a parameter that can be used to characterize the susceptibility of a given flip-flop to transients. It is readily measured, as described above. If published by chip manufacturers, it could be used by designers to estimate the probability of failure of a given circuit. This information is useful in the design stage, as well as in product testing. For example, ESD resting often involves repeated application of ESD pulses to the device under test. A knowledge of the probability of failure provides a sound basis for determining the number of tests required.

V. Conclusion

The results of an experimental study of the susceptibility of a D-type flip-flop to radiated transient electromagnetic interference have been reported. A transient impulse was used to simulate the radiated field produced during an ESD event. The study concentrated on dynamic failures, using a synchronized disturbance signal inductively coupled to the device under test.

The test results revealed that the flip-flop is susceptible only during specific time intervals within an operational cycle, and that the widths of these time intervals are dependent on the amplitude of the disturbing signal current. For TTL components, susceptibility is also dependent on the logic state of the data input line and on the implementation technology of the chip. CMOS chips showed very little variation with implementation technology. In general, the highest bandwidth chips begin to fail at the lowest disturbance current amplitudes, and vice versa. That is, bandwidth and susceptibility are inversely related.

A "susceptibility window" has been defined, and is proposed as a suitable parameter for assessing the probability of failure in a given situation. Such a parameter can be measured and could be quoted by component manufacturers.

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RF Characterization of The Semiconductor Junction Igniter in the 2.75 Folding Fin Aircraft Rocket

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***Abstract*—The design and characterization of a novel passive ignition system which consists of a simple two-stage radio frequency (RF) low pass filter and a novel RF insensitive electro-explosive device is discussed [1]–[3]. Lumped parameter modeling was used to provide the frequency response of the circuit. The 2.75 Folding Fin Aircraft Rocket (2.75 FFAR) was utilized as a test vehicle for field measurements which were performed as specified in MIL-STD 1385B at the Naval Surface Warfare Center in Dhalgren, VA. The configuration exhibited excellent performance over the entire frequency range of 1.5 MHz to 1 GHz.**

I. Introduction

Previous work reported in this journal demonstrated a high attenuation RF filter utilized in conjunction with a diode array. The filter assembly was capable of eliminating coupled RF signals between frequencies of 4–30 MHz and at 225 and 450 MHz in a 2.75 Folding Fin Aircraft Rocket (FFAR). (A complete discussion of the rocket and filter is contained in [3]).

The previously discussed approach required large numbers of ferrite beads as well as numerous stages of filtering due to the extremely high voltages which may be encountered on a Naval surface ship [3]–[5]. It is desirable to eliminate numerous components of the previous design. The reduction would result in a more simple, reliable and overall robust configuration.

This goal was made possible by the utilization of a RF insensitive electro-explosive device, the semiconductor junction igniter (SJI), as a replacement for the inherently sensitive bridgewire type presently in use [1].

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