Susceptibility Mapping [1]

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Abstract

The concept of susceptibility mapping is introduced. A susceptibility map is created by scanning a signal source (loop antenna) over a circuit board, and at each point raising the signal level until failure occurs. Maps obtained with CW EMI reveal design problems such as tight circuit timing or small static noise margins. They also reveal manufacturing problems, such as bad contacts and faulty chips. This leads to the concept of electromagnetic stress testing. Maps obtained with transient EMI require tight synchronization for repeatability and are useful in studying specific software-dependent failures.

1 Introduction

The immunity of digital circuits to various sources of electromagnetic interference is receiving increasing attention from digital equipment manufacturers. The need for improved immunity to EMI arises, in part, from the proliferation of sources of interference and the associated need for inter-operability of equipment such as computers, telephones, FAX machines, etc. A threat to the reliability of such equipment caused by increased electromagnetic interference would have devastating economic consequences, and in some cases can be life threatening. Another important impetus for the study of EMI immunity is that digital devices much faster than those currently in use are expected in the near future. Because of their wider bandwidth, faster devices are more susceptible to high-frequency radio signals and fast rise-time transients. A commonly encountered example of such transients is human electrostatic discharge, which involves currents having a rise-time in the range 100 ps to 1 ns. The spectral components of these fast pulses are well within the bandwidth of digital devices that operate at 100 MHz and above. Hence, susceptibility to the interference created by electrostatic discharge and by other sources operating in the gigahertz range is of considerable concern.

In this paper we describe a device that has been developed to record a susceptibility map for a digital circuit board. We demonstrate that such a map is a useful research tool in the study of immunity to EMI and that it can provide valuable information to the circuit designer and manufacturer. The results of several investigations that have been initiated as a result of studying susceptibility maps are reported in companion papers.

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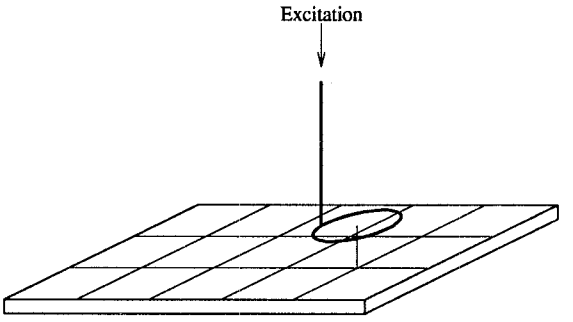

Figure 1: Antenna positioning for circuit board susceptibility mapping.

2 Susceptibility Mapping

The concept of field mapping is widely used for studying electromagnetic emissions from a circuit board. Commercial devices are available for capturing the emissions map and displaying it in the form of a surface plot or a contour plot. A susceptibility map is similar to an emissions map in that it gives a field value for each point on the board. However, the value on the susceptibility map gives the field intensity that if coupled to the board at that point would cause the board to malfunction.

A susceptibility map is obtained by scanning a suitable small antenna, such as a loop antenna, over a grid covering the board under test, as shown in Fig. 1. At each point of the grid, a localized interfering field is applied and the board operation is tested. The strength of the interfering signal is raised until the circuit fails. An example of a susceptibility map of a 6809 microprocessor board is shown in Fig. 2. The vertical axis in this figure represents susceptibility on a dB scale; higher points on the surface plot represent board areas where failure occurred at lower values of antenna current. In this test, single-frequency (CW) interference was used. It is also possible to use pulsed (transient) interference, as will be described later.

Peaks in the map reveal areas on the board that are most susceptible to an external EMI field. High susceptibility may be due to strong coupling caused by long wires or large loops on the board, or it may be due to a particularly sensitive device or signal path.

2.1 Antenna Design

The type, orientation and proximity to the board of the antenna used to apply the interfering field are important param-

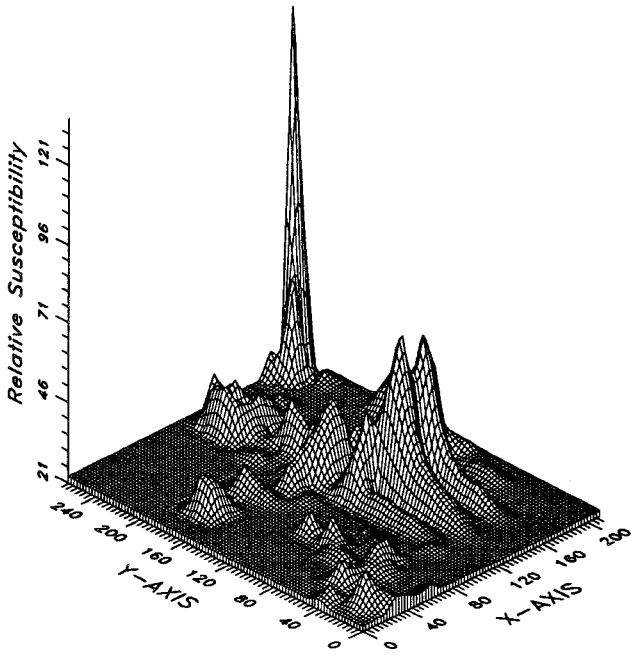

Figure 2: Susceptibility map of a 6809 microcomputer board for CW interference at 66.3 MHz.

eters of the susceptibility mapping procedure. The field should be limited to a small area underneath the antenna to obtain a high resolution. On the other hand, if the illuminated area is too small, large antenna currents are needed to produce a coupled signal of sufficient amplitude to cause failure. It was found experimentally that a 2.5-cm loop antenna oriented parallel to the board and at a distance of about 0.5 cm from the board provides the best trade-off between resolution and power requirements, for typical printed-circuit board wire spacings. Because of the close spacing from the board, the antenna is scanned over the solder side, which is free of protruding circuit components.

With the plane of the antenna loop parallel to the board, coupling takes place through the magnetic field component and is independent of the orientation of the wires on the board. The coupled disturbance signal can be represented by a voltage source and an inductive impedance in series with the circuit wiring. An alternative arrangement is to place the plane of the loop normal to the board. This leads to higher resolutions, but requires significantly higher antenna current. Again, coupling is effected by the magnetic field from the side of the loop lying closest to the board, and the coupling is strongest to nearby parallel conductors. Hence, the board must be scanned twice, once for each of two perpendicular orientations of the loop, to test all the board wiring.

The design of the loop antenna itself is shown in Figure 3. It is constructed from a thin, rigid 50-Ω coaxial cable. A balanced configuration is used so that no current flows on the outer conductors of the feed cables, making the loop the only radiating (or coupling) element. A second cable enables

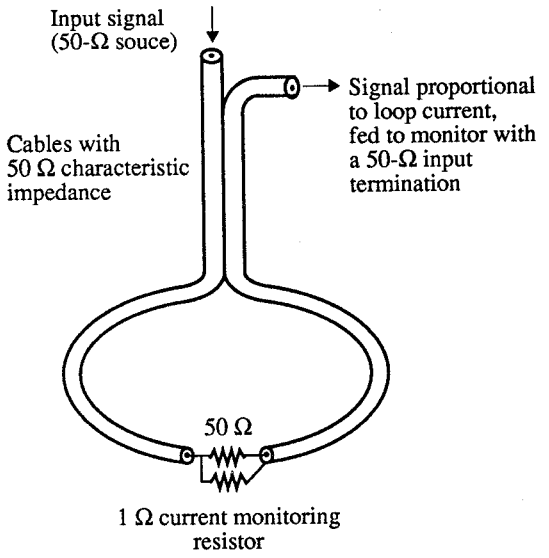

Figure 3: A balanced loop antenna with a current monitoring port.

monitoring of the loop current by picking up the voltage across a 1 Ω resistor in series with the loop. Current monitoring is necessary because for a given signal applied to the antenna, the antenna current, hence the magnetic field strength, is affected by the circuit under test. An additional resistor (50 Ω in Figure 3) governs the sensitivity of the monitoring circuit, in this case feeding 1% of the loop current to the monitor.

3 Experimental Results

One of the primary goals of our research program on electromagnetic compatibility is to achieve a better understanding of the ways in which EMI causes failures in digital circuits, with the ultimate objective of developing appropriate mitigation techniques. Susceptibility mapping proved to be a very effective tool for identifying various failure mechanisms.

Susceptibility maps were obtained for a 6809 microprocessor board under a variety of conditions. In most tests, a CW interference signal was used, and the map in Figure 2 is typical of the results obtained. Some of the failure mechanisms that were identified as a result of studying this and other maps are discussed briefly below. A more detailed discussion can be found in the references cited.

3.1 Oscillator Failure

The highest peak in Figure 2 is in the vicinity of the crystal oscillator that generates the main clock signal on the board, suggesting that the oscillator circuit may be highly susceptible to EMI. Because of this observation, the effect of an interfering signal on an oscillator circuit was examined in detail. The study revealed that an interfering signal can cause the oscillator to switch to a quite different frequency of oscillation, hence causing a complete loss of board function. Often, the

parasitic oscillation is stable in the sense that it continues after removal of the EMI, necessitating complete reset for restoration of board function.

Frequency switching was demonstrated in circuit simulations. An analytical model was also developed which predicted this behaviour and the values of the oscillator circuit parameters for which it can occur [1,2].

3.2 Repeatability

Repeated testing of the 6809 board showed that the susceptibility maps obtained in different tests were not identical. Occasionally, the failure thresholds at certain points on the board varied significantly from one test to another. Investigation of the sources of this mapping variability led to several discoveries about the nature of EMI-induced failures.

Positioning Accuracy

Initially, it was suspected that the accuracy of the positioning of the antenna over the board was an important factor. However, the same degree of variability was observed when tests were repeated at the same point without moving the antenna. The mechanical error in antenna positioning is less than 0.5 mm, which is small compared to the physical dimensions involved. Little change in the failure threshold was observed when the antenna was moved 1 or 2 mm.

Defective Components

Tests on several boards uncovered the existence of defective chips and bad contacts in some socketed components. In both cases, the board functioned correctly in the absence of interference. Clearly, these defects by themselves were not sufficient to cause malfunction. They only reduced the operational margins of the boards. With the added stress of EMI, the boards began to fail. When these problems were rectified, the repeatability of the susceptibility maps improved significantly.

The way in which EMI causes failures in the presence of chips with marginal operating parameters can be explained as follows. Logic gates are characterized by their drive capabilities and noise margins. A chip with a reduced noise margin, perhaps because of inadequate drive capability, is likely to cause a circuit failure at lower levels of EMI when compared to another chip that is fully within specification. A similar behaviour can be observed when the propagation delay of a logic gate is marginally out of specification. The effect of EMI on propagation delay is discussed later.

The link between EMI and bad contacts is not yet completely understood. It is suspected that bad contacts act as rectifying junctions which change the DC level of the logic signals in the presence of EMI, and thus also change the noise margin. It is also possible that the currents induced by EMI cause a marginal contact to break down completely. This phenomenon requires further investigation.

Frequency Sensitivity

A certain amount of variability in the susceptibility map remained after replacing the defective chips and bad contacts. Further investigation revealed that frequency instability of the interference source (built into a network analyzer) was a major contributor to this variability. Figure 4 gives the failure threshold as a function of frequency at a point on the board near the main oscillator. The figure shows that the failure threshold changes rapidly with frequency for certain frequencies. Similar curves, but with less pronounced dips, were obtained for other points on the board. When a highly stable frequency source (synthesizer) was used to generate the EMI signal, the repeatability of the results became well within the experimental measurement error.

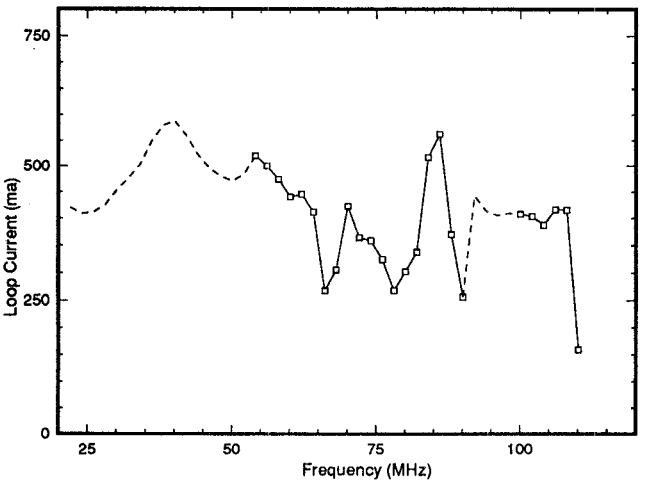

Figure 4: Failure threshold as a function of frequency at a point near the susceptibility peak in Fig. 2

The effect of the frequency of the interfering signal on failures can be readily attributed to the fact that both the field coupling and the failure modes of the circuit are frequency dependent. The strong sensitivity to frequency seen at certain frequencies in Figure 4 is likely due to resonance phenomena. Resonance can occur both in the field coupling and in the failure mechanism. The strength of the interference signal induced in a transmission line by an incident field can exhibit resonance characteristics when the line length is of the order of $\lambda/4$. At 60 MHz and for typical PC board materials, only the longest wires on a board would be likely to show resonance effects.

The oscillator frequency switching phenomenon described earlier is an example of a failure mechanism with resonance characteristics. The oscillator used on the board under test has a fundamental frequency of 22.1 MHz, which is determined by a quartz crystal. Due to the circuit's nonlinearities, stable oscillations occurred at 55 MHz for one of the oscillators tested. The oscillator switches to this frequency when an interference signal is applied with a frequency close to 55 MHz or to one of the harmonics of the crystal. Hence, the board showed increased susceptibility at these frequencies.

Another frequency-dependent failure mode is that of EMI-induced changes in the propagation delay of the logic signal, which is discussed below. However, in that case, no resonance behaviour has been identified.

3.3 Induced Delay

It was observed by several researchers that CW electromagnetic interference causes a change in the timing of logic transitions [3]. This effect was studied in detail to determine its contribution to the differences in failure threshold at different locations on the board under test. A model was developed to predict the EMI-induced change in propagation delay for a given interference signal [2,4]. It was shown that these induced delays are the primary cause of circuit failure at low levels of EMI, and that increased immunity can be achieved when these delays are properly accounted for in the circuit's design [5,6].

The fact that an injected interference signal causes a change in signal timing, combined with the diagnostic capability referred to earlier, gave support to the concept of electromagnetic stress testing presented below.

3.4 Transient Mapping

The experimental results reported above were all obtained using CW interference signals. Susceptibility mapping was also examined using transient interference pulses that approximate the current waveform of a human electrostatic discharge. Since a failure caused by a transient pulse is dependent on the timing of that pulse relative to the events on the circuit board, repeatable results require the pulse to be synchronized to a particular event on the board. Thus, transient-induced failures are software-dependent. Several series of tests were conducted in which the pulse was synchronized to memory read and write operations. This led to software-dependent susceptibility maps in the vicinity of the board's memory chips, which in turn led to an investigation of the failure modes of storage elements subjected to transient interference. Experimental results for different types of flip-flops showed the existence of a *failure window* similar to but wider than the setup-hold window [7]. Transient interference pulses occurring within the failure window may cause the flip-flop to malfunction.

4 Electromagnetic Stress Test

It has been shown above that an interference signal injected into a circuit board, by whatever means, will interact with the circuit components in a variety of ways, and may cause the circuit to malfunction. These interactions form the basis for a diagnostic tool that can be used by researchers in the field, as well as by the designers and manufacturers of digital circuits. A scanning device of the type described in this paper can be used to obtain the susceptibility map of a circuit board. For the circuit designer, this map provides information on the sensitivity of various parts of the circuit to small changes in voltage levels and propagation delays. Thus, critical paths that are close to their operational limits can be easily identified.

Circuit manufacturers can make use of the ability of this test to detect marginal components and bad contacts. By comparing the map of a new board to a known reference, defective boards can be identified. Boards containing marginal components are likely to exhibit intermittent faults, which are often difficult to detect. Thus, a similar approach can be used to test circuit boards returned from the field for repair.

The electromagnetic stress test is similar to other forms of stress testing, such as those involving the use of high temperature, humidity, or mechanical vibrations. The means by which the interfering signal is injected need not be limited to magnetic coupling through an antenna. A capacitive probe could be used as well. Moreover, direct coupling to specific points in a circuit may be beneficial in many cases. The ability to inject an interfering signal would be a particularly useful feature if incorporated in logic analyzers. This would allow circuit designers to test their designs experimentally, not just through simulation, to asses the effects of changes in the propagation delay of various components.

5 Conclusions

The concept of susceptibility mapping has been introduced, and has been shown to be a useful tool for examining the failure modes of a digital circuit subjected to electromagnetic interference. The issue of repeatability of results proved to be a key for understanding the main parameters that affect the resulting maps. Susceptibility mapping led to the concept of electromagnetic stress testing, which can be used by the designers, manufacturers and users of digital circuit boards.

Acknowledgment

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6 References

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