UNIVERSITY OF TORONTO
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

ECE424F Microwaves

Experiment: **A 1GHz Microstrip Solid-State Amplifier**

1. Purpose

The purpose of this experiment is to design, build and test a 1GHz transistor amplifier for maximum gain. The amplifier will be constructed in microstrip technology. The experiment consists of two parts. In part I the amplifier will be designed using Puff and the Smith chart. In part II, the designed amplifier will be constructed, tuned and characterized using a Scalar Network Analyzer and a Sweep Generator.

2. Theoretical Background

2.1 Transistor Amplifier Design

The generic block-diagram of a single-stage transistor amplifier is shown in Fig. 1. The transistor is characterized as a linear two-port by means of four scattering parameters. The scattering parameters are usually given by the manufacturer as a function of the frequency for various DC operating points. The specification sheets for the bipolar transistor to be used in this experiment are attached as an Appendix. To achieve maximum gain, the matching networks (see Fig. 1) should be designed so that conjugate matching is achieved at the input and output ports of the transistor. For the purposes of this experiment, the matching networks will be optimized at 1GHz for a class A transistor configuration. This leads to narrow band characteristics.

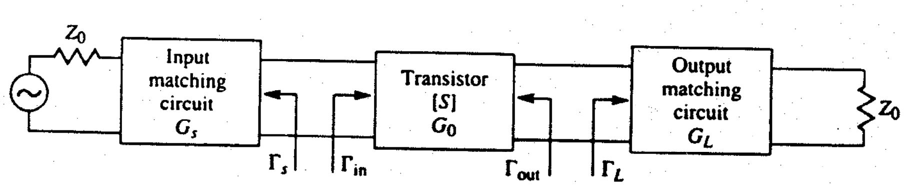


Figure 1

2.1.1 Stability

The network of Fig. 1 is said to be unconditionally stable if $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ for ALL passive source and load impedances. If the network is not stable then the amplifier becomes an oscillator. To ensure unconditional stability the following necessary and sufficient conditions should be satisfied:

$$\mathbf{K} = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \quad \text{and} \quad \Delta = S_{11}S_{22} - S_{12}S_{21} < 1$$

2.1.2 Design for maximum gain

The transducer power gain $G_T = P_{L,av} / P_{av}$ for the amplifier of Fig.1 is defined as the ratio of the power available from the two-port network to the power available from the source. To achieve maximum transducer power gain both the input and output ports should be conjugately matched i.e. $\Gamma_{in} = \Gamma_S^*$ and $\Gamma_{out} = \Gamma_L^*$. In this case, the maximum transducer power gain is given by:

$$G_{T,max} = \frac{1}{1 - |\Gamma_S|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2}$$

The corresponding necessary input and output reflections coefficients which determine the matching networks are given by:

$$\Gamma_S = \frac{B_1 \pm \sqrt{B_1^2 - 4|C_1|^2}}{2C_1} \quad \text{and} \quad \Gamma_L = \frac{B_2 \pm \sqrt{B_2^2 - 4|C_2|^2}}{2C_2}$$

where

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2$$
$$B_1 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2$$

$$C_1 = S_{11} - \Delta S_{22}^*$$
$$C_2 = S_{22} - \Delta S_{11}^*$$

3. Amplifier Circuit Topology

The topology of the amplifier to be constructed is shown in Fig. 2. As shown, microstrip double-stub tuners are used to realize the input and output matching networks. The advantage of this type of matching circuit is that it can be easily tuned by trimming the open stubs to match the transistor to the external system. However, the disadvantage (compared to single-stub tuning for example) is that the matching network is large resulting to higher conductor losses. Therefore, this kind of matching circuitry is not often used in low-noise amplfier design.

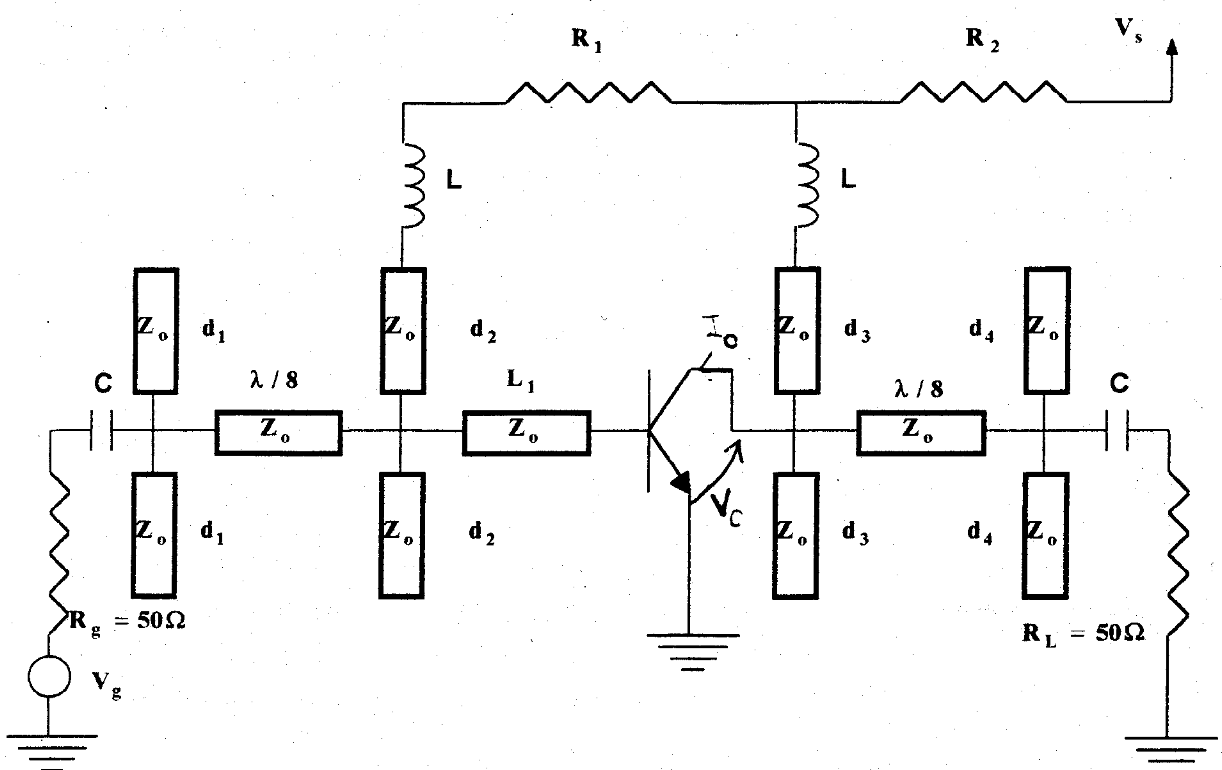


Figure 2.

4. Part-1: Design the Amplifier

All transmission line parameters are at an impedance level of $Z_0 = 50\Omega$. For the substrate, assume a relative permittivity of $\varepsilon_r = 4.0$.

1. Calculate the biasing resistors $\mathbf{R_1}$ and $\mathbf{R_2}$ for an operating point of $\mathbf{I_0 = 10mA}$ and $\mathbf{V_0 = 10V}$ at $\mathbf{V_s = 24V}$. Assume that the DC current gain $\mathbf{h_{FE} = 100}$. For these bias conditions, the corresponding S-parameters in the range $\mathbf{0.1GHz \le f \le 2GHz}$ are stored in the file Mrf901 under your Puff directory. Subsequently, the device can be invoked from puff as a two port by the command line

   device Mrf901

2. Calculate the stability factors $\mathbf{K}$ and Δ at 1GHz. Is the transistor stable ?

3. What is the theoretical maximum transducer gain of the amplifier ?

4. It is given that $\mathbf{L_1 = 0.153\lambda}$ (where λ denotes the microstrip-mode guided wavelength). Design the input and output double-stub matching networks for maximum transducer gain, i.e. determine $\mathbf{d_1}$, $\mathbf{d_2}$, $\mathbf{d_3}$ and $\mathbf{d_4}$. It is strongly recommended to use Puff, but you can use the Smith chart if you so wish. A helpful feature of Puff is that of single-variable optimization. That is, if you wish to sweep a variable (say the equivalent phase shift of a transmission line) then the question mark symbol **?** should be placed in front of the swept variable. For example, **a tline 50Ω ?20°**, sweeps the electrical length of transmission line ,a, between the limits specified on the axes of the rectangular plot. When the circuit is analyzed from the plot-window, the response will be a function of the swept variable rather than the frequency. Note that only one variable can be swept at a time. Furthermore, a lumped impedance can be specified by the statement "lumped", for example: **lumped 30 + 20j Ω**. To connect the lumped impedances to the ground use the "=" key while in the layout window. Another helpful feature of Puff is that you can switch between impedance and admittance coordinates on the displayed Smith chart by using the Tab-key. This is useful since you have to work with shunt stubs.

5. What should the decoupling capacitor ,C, be if $\mathbf{X_c} = \mathbf{0.5\Omega}$ at 1GHz ?

6. What should the RF-choke inductance ,L, be if $\mathbf{X_l} = \mathbf{10K\Omega}$ at 1GHz ?

7. With the aid of the information given in the Appendix, draw a 1:1 microstrip layout of the matching network at 1GHz .

8. Construct your matching networks using the provided PC-board substrate, the suitable width draft-tape and the scotch tape.

5. Part-2: Constructing and Testing the Amplifier

Construct the bias network:

1. Using the given iron-cores and enameled wire wind the two choke inductors ,L. These choke inductors ensure that no microwave-power leaks to the biasing network. Solder the chokes in place.

2. Continue by soldering the biasing resistors $\mathbf{R_1}$ **and** $\mathbf{R_2}$ in place.

3. Follow the procedure in the Appendix for soldering the provided decoupling chip-capacitors.

Tune the matching networks

1. Calibrate the scalar network analyzer.

2. Set the bias voltage to $\mathbf{V_s} = \mathbf{24V}$ and measure the input and output reflection coefficients (i.e. including the matching networks). Trim the open circuit stubs until you achieve near matching conditions at 1GHz.

Measuring the forward and reverse gains

1. Calibrate the scalar network analyzer with the attenuator inserted between the HP bridge and the detector.

2. Measure the forward $\mathbf{G_T}$ and reverse gain $\mathbf{G_R}$ as a function of the frequency between 0 and 2GHz. What are the gain values at 1GHz ?

6. Discussion

Compare the measured reflection coefficients and gains with the simulate/computed ones. How close the two are ? Why is the gain of the amplifier lower than calculated ?

What is the bandwidth of the amplifier (assuming that at least 0dB of gain is achieved) ?

Bias

COLLECTOR DC FEED BOARD

ut Board
iginal.

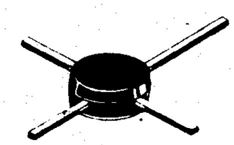
MRF901

The RF Line

2.5 dB @ 1.0 GHz

HIGH FREQUENCY TRANSISTOR

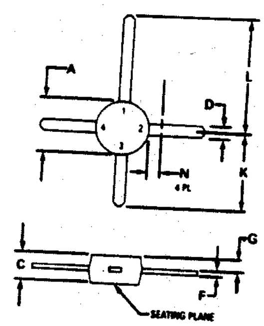
NPN SILICON



NPN SILICON HIGH-FREQUENCY TRANSISTOR

. . . designed primarily for use in high-gain, low-noise small-signal amplifiers. Also usable in applications requiring fast switching times.

- High Current-Gain-Bandwidth Product — f_T = 4.5 GHz (Typ) @ I_C = 15 mAdc
- Low Noise Figure @ f = 1.0 GHz — NF = 2.0 dB (Typ) and 2.5 dB (Max)
- High Power Gain — G_{pe} = 10 dB (Min) @ f = 1.0 GHz
- Third Order Intercept = +23 dBm (Typ)



STYLE 2
PIN 1 COLLECTOR
2 EMITTER
3 BASE
4 EMITTER

NOTE
DIMENSION D NOT APPLICABLE IN ZONE N

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.84	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.76	1.14	0.030	0.045
K	7.24	8.13	0.285	0.320
L	10.54	11.43	0.415	0.450
N	—	1.65	—	0.065

CASE 317-01

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	25	Vdc
Emitter-Base Voltage	V_{EBO}	2.0	Vdc
Collector Current — Continuous	I_C	30	mA
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	0.375 3.3	Watt mW/°C
Storage Temperature Range	T_{stg}	150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	300	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	15	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	25	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	2.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	50	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	30	80	200	–
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwith Product (I_C = 15 mAdc, V_{CE} = 10 Vdc, f = 1.0 GHz)	f_T	–	4.5	–	GHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	0.4	1.0	pF
Noise Figure (I_C = 5.0 mAdc, V_{CE} = 6.0 Vdc, f = 1.0 GHz)	NF	–	2.0	2.5	dB
FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 6.0 Vdc, I_C = 5.0 mA, f = 1.0 GHz)	G_{pe}	10	12	–	dB
Third Order Intercept (I_C = 5.0 mAdc, V_{CE} = 6.0 Vdc, f = 0.9 GHz)	–	–	+23	–	dBm

FIGURE 1 — 1.0 GHz TEST CIRCUIT SCHEMATIC

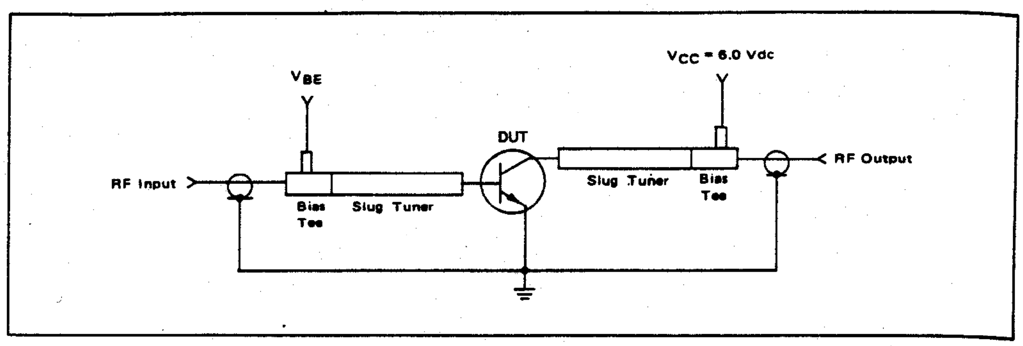
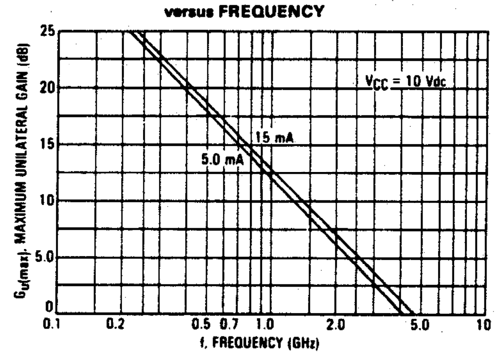


FIGURE 2 — MAXIMUM UNILATERAL GAIN versus FREQUENCY



Max	Unit
–	Vdc
–	Vdc
–	Vdc
50	nAdc
200	–
–	GHz
1.0	pF
2.5	dB
–	dB
–	dBm

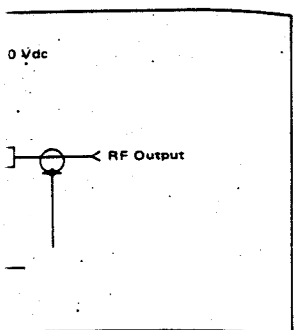


FIGURE 3 — CURRENT GAIN — BANDWIDTH PRODUCT versus COLLECTOR CURRENT

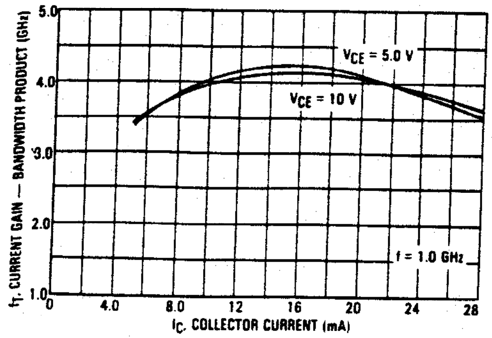


FIGURE 4 — NOISE FIGURE versus FREQUENCY

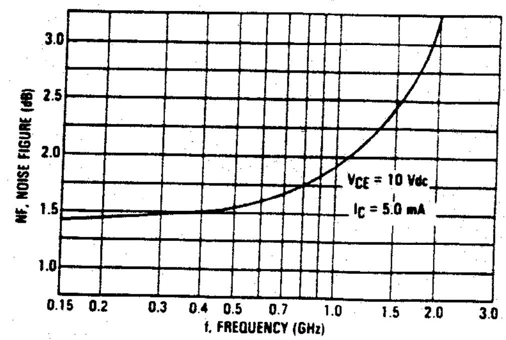


FIGURE 5 — NOISE FIGURE versus COLLECTOR CURRENT

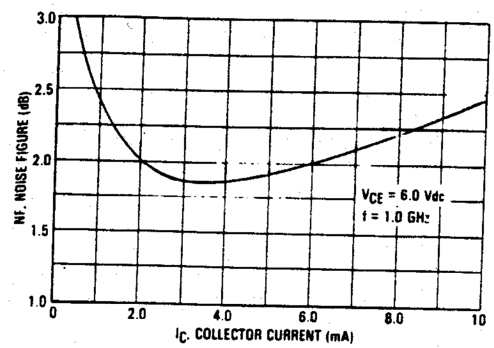


FIGURE 6 — MAXIMUM UNILATERAL GAIN versus COLLECTOR CURRENT

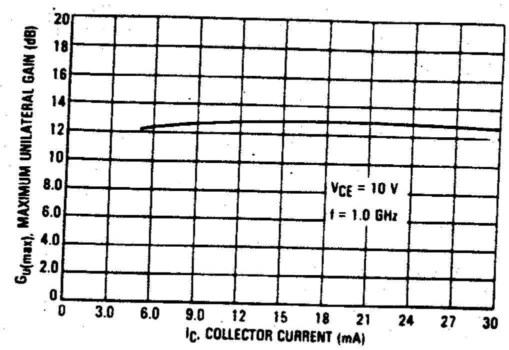


FIGURE 7 — $|S_{21}|^2$ versus FREQUENCY

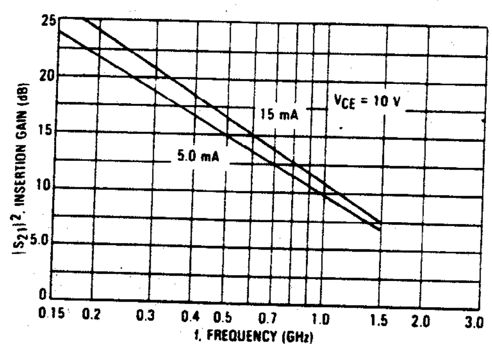
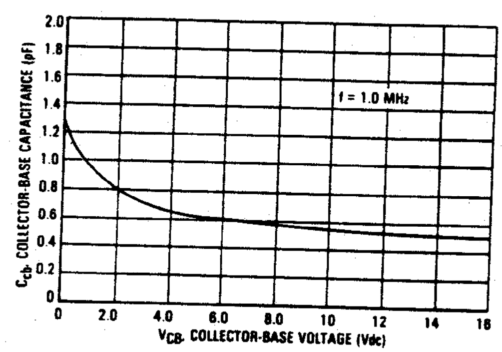


FIGURE 8 — COLLECTOR-BASE CAPACITANCE versus COLLECTOR-BASE VOLTAGE



2 2

TABLE I

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11} $\lvert S_{11}\rvert$	S_{11} $\angle\phi$	S_{21} $\lvert S_{21}\rvert$	S_{21} $\angle\phi$	S_{12} $\lvert S_{12}\rvert$	S_{12} $\angle\phi$	S_{22} $\lvert S_{22}\rvert$	S_{22} $\angle\phi$
5.0	5.0	100	0.71	-38	11.30	153	0.03	68	0.92	-17
		200	0.62	-75	9.48	133	0.05	55	0.76	-29
		500	0.54	-141	5.40	100	0.07	43	0.48	-44
		1000	0.53	178	2.93	76	0.09	48	0.40	-56
		2000	0.59	130	1.51	48	0.16	62	0.35	-85
	10	100	0.57	-58	16.95	145	0.03	63	0.85	-23
		200	0.51	-103	12.61	123	0.04	53	0.64	-35
		500	0.52	-161	6.24	93	0.06	50	0.38	-45
		1000	0.52	166	3.24	73	0.09	61	0.33	-54
		2000	0.59	125	1.66	47	0.17	67	0.29	-84
	15	100	0.48	-75	20.08	139	0.02	61	0.80	-27
		200	0.47	-121	13.89	117	0.04	53	0.57	-38
		500	0.53	-170	6.44	91	0.05	56	0.34	-44
		1000	0.53	162	3.33	72	0.09	66	0.31	-52
		2000	0.60	123	1.70	46	0.18	68	0.28	-82
	20	100	0.44	-88	21.62	136	0.02	60	0.76	-28
		200	0.47	-132	14.33	114	0.03	54	0.53	-38
		500	0.53	-175	6.45	89	0.05	60	0.32	-41
		1000	0.53	159	3.31	70	0.09	68	0.31	-50
		2000	0.61	122	1.69	45	0.18	70	0.28	-80
	30	100	0.43	-112	21.45	130	0.02	58	0.72	-28
		200	0.50	-148	13.38	109	0.03	57	0.51	-33
		500	0.57	178	5.82	86	0.05	65	0.35	-34
		1000	0.57	156	2.99	68	0.08	73	0.35	-46
		2000	0.65	121	1.50	42	0.18	74	0.33	-78

TABLE II

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11} $\lvert S_{11}\rvert$	S_{11} $\angle\phi$	S_{21} $\lvert S_{21}\rvert$	S_{21} $\angle\phi$	S_{12} $\lvert S_{12}\rvert$	S_{12} $\angle\phi$	S_{22} $\lvert S_{22}\rvert$	S_{22} $\angle\phi$
10	5.0	100	0.73	-35	11.32	154	0.03	69	0.93	-14
		200	0.63	-69	9.69	135	0.05	57	0.79	-25
		500	0.53	-135	5.65	101	0.07	43	0.54	-38
		1000	0.51	-177	3.11	77	0.08	50	0.47	-48
		2000	0.57	132	1.58	48	0.14	66	0.41	-75
	10	100	0.59	-52	17.06	147	0.02	64	0.87	-19
		200	0.52	-95	13.06	125	0.04	54	0.69	-30
		500	0.49	-156	6.58	95	0.05	51	0.45	-37
		1000	0.50	170	3.44	74	0.08	62	0.41	-45
		2000	0.57	126	1.75	47	0.16	70	0.36	-72
	15	100	0.51	-66	20.36	141	0.02	63	0.83	-22
		200	0.47	-112	14.48	119	0.03	54	0.63	-31
		500	0.50	-166	6.81	92	0.05	57	0.41	-35
		1000	0.50	164	3.54	72	0.08	67	0.39	-43
		2000	0.58	124	1.78	46	0.16	72	0.35	-70
	20	100	0.47	-78	22.08	138	0.02	61	0.80	-23
		200	0.46	-123	15.07	116	0.03	55	0.60	-30
		500	0.50	-171	6.84	90	0.05	60	0.40	-32
		1000	0.51	162	3.51	71	0.08	69	0.39	-41
		2000	0.59	123	1.77	45	0.17	73	0.35	-68
	30	100	0.44	-98	22.70	133	0.02	59	0.76	-23
		200	0.47	-139	14.47	111	0.03	55	0.57	-27
		500	0.53	-177	6.33	87	0.04	65	0.43	-28
		1000	0.54	158	3.26	69	0.07	74	0.43	-39
		2000	0.62	122	1.61	42	0.16	77	0.39	-68

S_{12}	S_{22}	
∠φ	$\lvert S_{22}\rvert$	∠φ
68	0.92	-17
55	0.76	-29
43	0.48	-44
48	0.40	-56
62	0.35	-85
63	0.85	-23
53	0.64	-35
50	0.38	-45
61	0.33	-54
67	0.29	-84
61	0.80	-27
53	0.57	-38
56	0.34	-44
66	0.31	-52
68	0.28	-82
60	0.76	-28
54	0.53	-38
60	0.32	-41
68	0.31	-50
70	0.28	-80
58	0.72	-28
57	0.51	-33
65	0.35	-34
73	0.35	-46
74	0.33	-78

S_{12}	S_{22}	
∠φ	$\lvert S_{22}\rvert$	∠φ
69	0.93	-14
57	0.79	-25
43	0.54	-38
50	0.47	-48
66	0.41	-75
64	0.87	-19
54	0.69	-30
51	0.45	-37
62	0.41	-45
70	0.36	-72
63	0.83	-22
54	0.63	-31
57	0.41	-35
67	0.39	-43
72	0.35	-70
61	0.80	-23
55	0.60	-30
60	0.40	-32
69	0.39	-41
73	0.35	-68
59	0.76	-23
55	0.57	-27
65	0.43	-28
74	0.43	-39
77	0.39	-68

FIGURE 9 — INPUT AND OUTPUT REFLECTION COEFFICIENTS versus FREQUENCY (V_{CE} = 10 V, I_C = 15 mA)

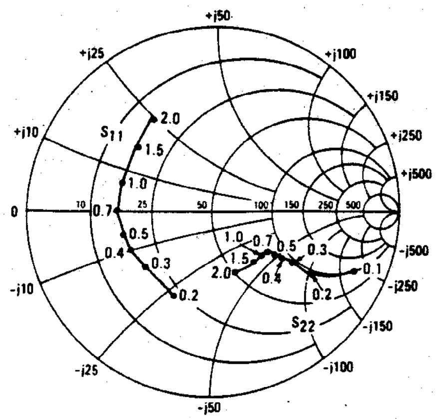


FIGURE 10 — FORWARD/REVERSE TRANSMISSION COEFFICIENTS versus FREQUENCY (V_{CE} = 10 V, I_C = 15 mA)

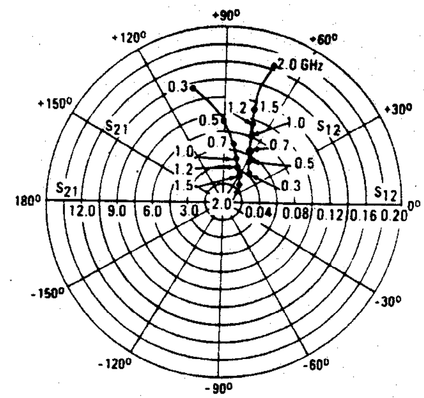
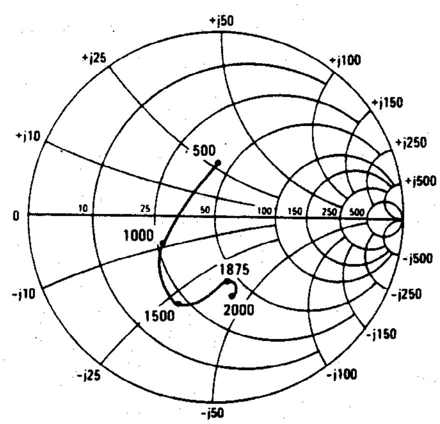
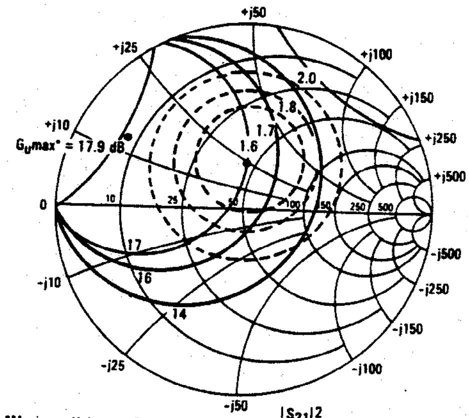


FIGURE 11 — SOURCE IMPEDANCE (Γms) FOR OPTIMUM NOISE FIGURE versus FREQUENCY (V_{CE} = 10 Vdc, I_C = 5.0 mA)



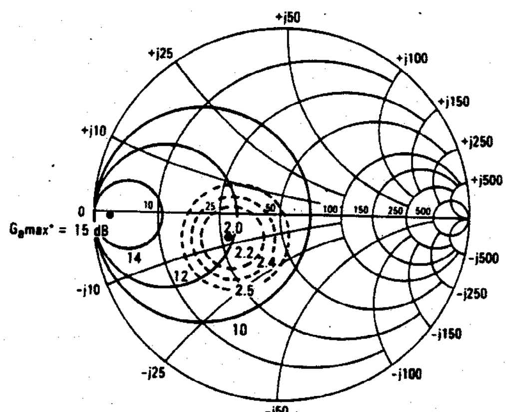
2

FIGURE 12 — CONSTANT GAIN AND NOISE FIGURE CONTOURS
(V_{CE} = 10 Vdc, I_C = 5.0 mA f = 500 MHz)



*Maximum Unilateral Gain, $G_u max = \frac{|S_{21}|^2}{(1 - |S_{11}|^2)(1 - |S_{22}|^2)}$ (K < 1)

FIGURE 13 — CONSTANT GAIN AND NOISE FIGURE CONTOURS
(V_{CE} = 10 Vdc, I_C = 5.0 mA f = 1.0 GHz)

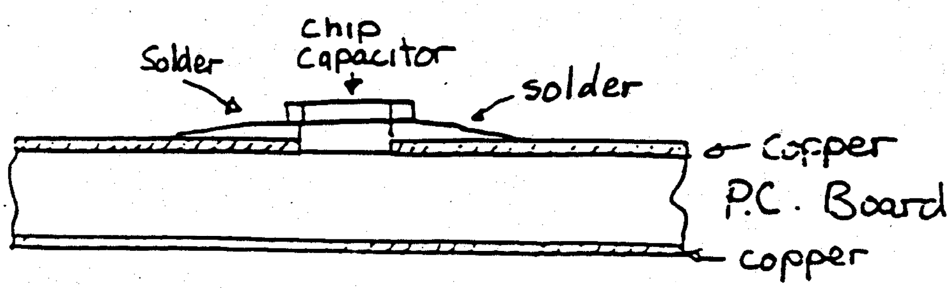


*Maximum Available Gain, $G_a max = \frac{|S_{21}|}{|S_{12}|}(K \pm \sqrt{K^2 - 1})$ (K > 1)

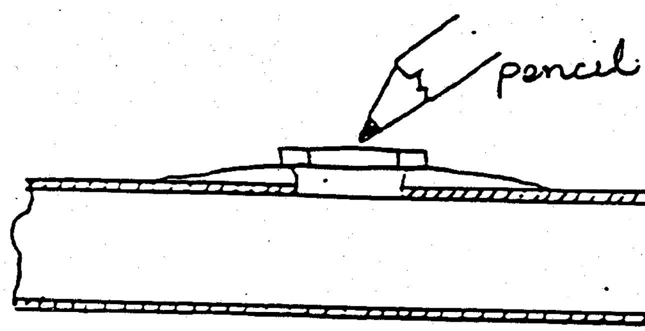
SOLDERING PROCEDURE FOR CHIP CAPACITOR:

1. Tin microstrip ends where capacitors are going to be located.

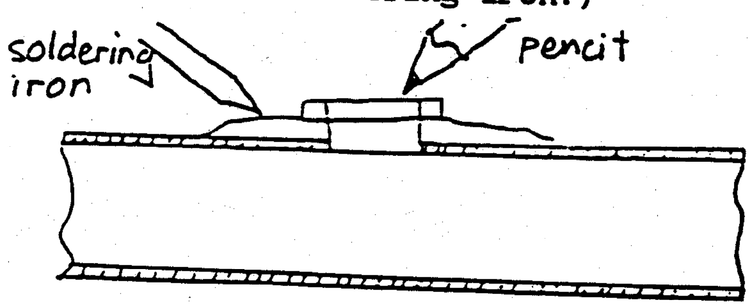
2. Place cap on top of solder as shown below:



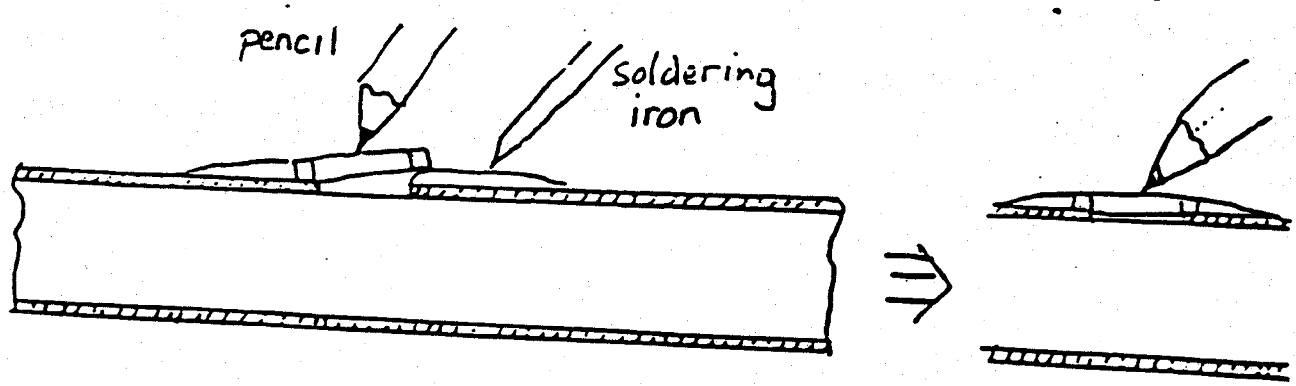
3. Hold down with pencil.



4. Place soldering iron tip onto solder beside the cap. (Do not touch cap with soldering iron.)



5. Wait until solder melts and cap drops. Then remove soldering iron immediately and repeat 4 and 5 on the other side right away.



MICROSTRIP DESIGN TECHNIQUES FOR UHF AMPLIFIERS

Prepared by:
Glenn Young

INTRODUCTION

This note uses a 25 watt UHF amplifier design as a vehicle to discuss microstrip design techniques. The design concentrates on impedance matching and microstrip construction considerations. A basic knowledge of Smith chart techniques is helpful in understanding this note.[1]

The amplifier itself, as shown in Figure 1, provides 25 watts of output power in the 450 - 512 MHz UHF band. It is designed for 12.5 volt operation which makes it useful for mobile transmitting equipment. A variety of police, taxi, trucking and utility maintenance communication systems operate in this band.

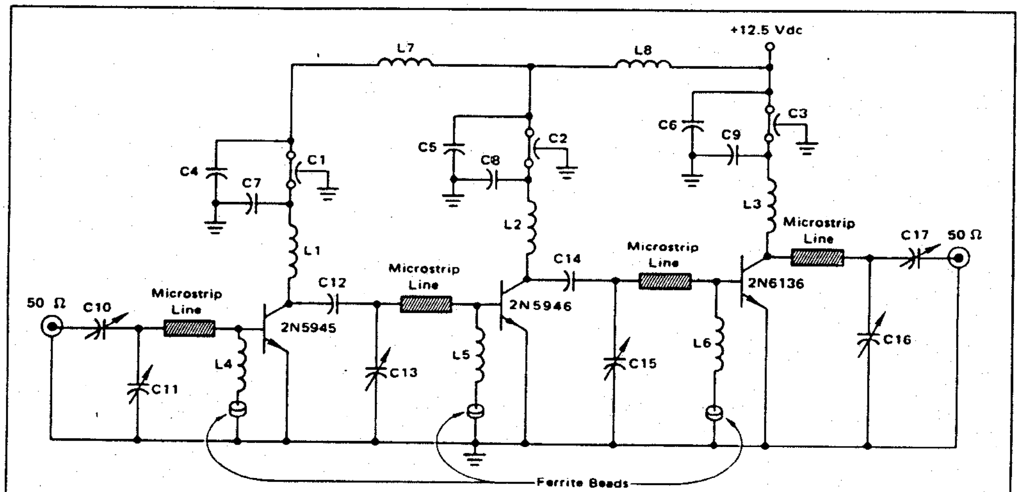
A summary of the performance of the completed amplifier operating with a 12.5 volt supply at 512 MHz indicates a power gain of 16 dB and a bandwidth (-1 dB) of 8 MHz. Overall efficiency is 48.5% and all harmonics are a minimum of 20 dB below the fundamental output.

Sections on construction and device handling considerations are also presented.

MICROSTRIP DESIGN CONSIDERATIONS

Microstrip design was used for this amplifier due to its inherent superiority over other methods at this frequency. These techniques not only offer good compatibility with the Motorola "stripline" package but they also offer very good reproducibility. Microstrip construction is more efficient than lumped constant equivalents since microstrip lines are less lossy than lumped constant components.

Microstrip board with Teflon bonded fiberglass dielectric rather than the higher dielectric constant ceramics was chosen due to the ease of working with that type of material. A substrate thickness of 1/16-inch is convenient since a line of the same width as the transistor leads (0.225 inch) produces a reasonable characteristic impedance (Z_O) of 40.65 ohms. The value of the characteristic impedance is



All Microstrip lines 5.72 mm wide 2.5 cm long
C1,2,3, 470 pf feedthru
C4,5,6 1.0 µf Tantalum
C7,8,9 0.1 µf Ceramic
C10,11,13,15,16,17 1.5-20 pf Compression Trimmer AHCO 420
C12,14 10 pf Microwave capacitor ATC type 100-B-10-M-MS or equiv.

L1, L2, L3 – 5 turns #20 Closewound 3/16" I.D.
L4, L5, L6 – 0.15 µh molded choke
L7, L8 – Ferroxcube VK 200 20/48 or equiv.
Ferrite beads are Ferroxcube 56 590 65/38 or equiv.

FIGURE 1 – Schematic Diagram of 25 W UHF Amplifier

calculated from:[4]

$$Z_o = \frac{377h}{\sqrt{\epsilon_r} \times W \left[1 + 1.735\,\epsilon_r^{-.0724}\left(\frac{W}{h}\right)^{-.836}\right]} \quad (1)$$

where ϵ_r = dielectric constant
W = width of microstrip line
h = thickness of the dielectric

The h term is equal to the total thickness of the microstrip board minus the thickness of the copper on both sides. In this design that term is equal to

$$h = 62 - (2 \times 1.4) = 59.2 \text{ mils}$$
$$1 \text{ oz. copper} = 1.4 \text{ mils thick} \quad (2)$$

The effective width should be used when the conductor is of finite thickness.

$$W_{eff} = W + \frac{t}{\pi}\left(\ln\frac{2h}{t} + 1\right) \quad (3)$$

where t = thickness of the conductor

$$W_{eff} = 225 + (1.4/\pi)\left(\ln\frac{2 \times 59.2}{1.4} + 1\right) = 227.4 \text{ mils}$$

therefore: (4)

$$Z_o = \frac{377 \times .0592}{\sqrt{2.5 \times .2274}\left[1 + 1.735 \times 2.5^{-.0724} \times \left(\frac{227.4}{59.2}\right)^{-.836}\right]} = 40.65\,\Omega \quad (5)$$

THE AMPLIFIER DESIGN

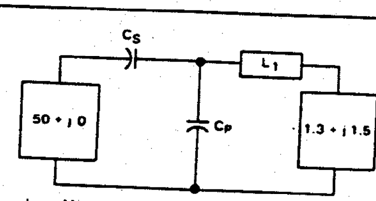
The first decision in the design was determining the type of matching networks to be used. The network shown in Figure 3 was chosen because of its ability to "map" a large area of complex impedances; this allows a good tuning margin to compensate for normal variations in transistor impedances and other peripheral effects. A side benefit of this network is that the series tuning element provides the dc blocking function, eliminating the need for coupling capacitors.

The synthesis of the matching networks utilizes the large signal impedances of the transistors as specified on the data sheets. These parameters should not be confused with small signal 2-port parameters. A complete discussion of large signal characterization is given in Motorola Application note AN-282A. The impedance parameters used in this note are taken from the respective data sheets and were obtained in the manner described in AN282A.

2N5945
Z_{in} 1.3 + j1.5 ohms
Z_{out} 4.6 - j5.4 ohms
2N5946
Z_{in} 1.3 + j1.2 ohms
Z_{out} 4.2 - j0.5 ohms
2N6136
Z_{in} 1.3 + j4.11 ohms
Z_{out} 3.2 + j1.96 ohms

FIGURE 2 – Transistor Complex Input and Output Impedance at 470 MHz (Series Form)

Smith chart techniques are used to synthesize the matching networks in the amplifier to be described. The complex series equivalent input and output impedances as taken from the data sheets are shown in Figure 2. There are an infinite number of solutions to the required matching networks, however, once an initial choice of one of the components is made, only one solution exists. It is obvious that all components need to be kept within reasonable limits, however it would seem that the most critical parameter is the length of the microstrip line. Using this assumption, the length of the line is chosen as a starting point. The input network, shown in Figure 3 will be solved to illustrate the technique.



L_1 = Microstrip Line 5.72 mm wide 2.5 cm long
C_S = 4.08 pF
C_P = 16.84 pf

FIGURE 3 – Equivalent Circuit of Input Network

Before proceeding to determine the component values, the effective wavelength of the desired frequency in the microstrip line must be known. This is accomplished by first finding λ_o, the wavelength in free space:

$$\lambda_o = \frac{c}{freq} = \frac{3 \times 10^8}{4.7 \times 10^8} = 0.638 \text{ meters} \quad (6)$$

where c = propagation constant, free space

The TEM mode wavelength is determined:

$$\lambda_{TEM} = \lambda_o/(\epsilon_r)^{1/2} = 63.8\text{cm}/(2.5)^{1/2} = 40.37\text{cm} \quad (7)$$

Now as the propagation in microstrip line is not pure TEM mode, a correction factor must be applied to the last calculation.[4]

$$K = \left[\frac{\epsilon_r}{1 + 0.63(\epsilon_r - 1)\left(\frac{W}{h}\right)^{.1225}}\right]^{1/2}$$
$$= \left[\frac{2.5}{1 + 0.63(2.5-1)(227.4/59.2)^{.1225}}\right]^{1/2} = 1.086 \quad (8)$$

Then:

$$\lambda' = (\lambda tem)(K) = (40.37)(1.086) = 43.85 \text{ cm} \quad (9)$$

This is the effective wavelength and will be used in all further calculations. Equation 8 is valid for width to height ratios of 0.6:1 or greater. For ratios less than 0.6:1 alter the (w/h) factor in the denominator to $(w/h)^{.0297}$

The source and load impedances must now be normalized to the 40.65Ω characteristic impedance of the line and

7

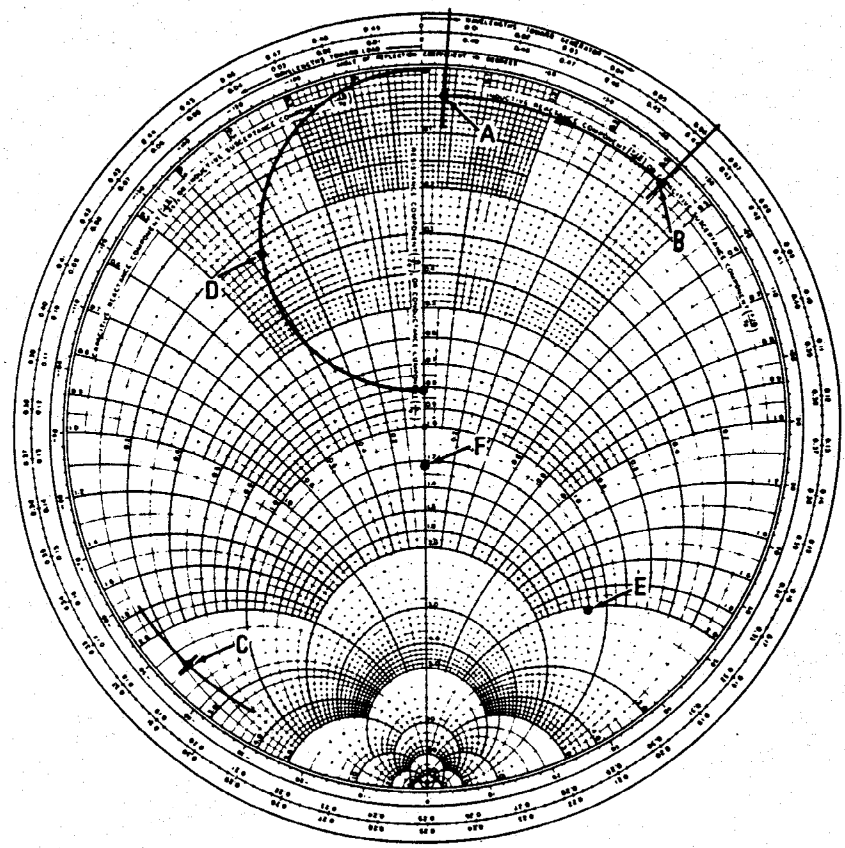


FIGURE 4 – Smith Chart Solution

plotted on the Smith chart. It should be noted that the terms "source" and "load" are used here only in reference to the Smith chart solution.

A source impedance of 50 + j0 is normalized to 1.23 + j0 and a load impedance of 1.3 + j1.5 is normalized to 0.032 + j0.0369. The load impedance is plotted at point A in Figure 4 and the source impedance at point F. An arbitrary choice of 2.5 cm for the line length was made. This is an electrical length of:

$$\text{electrical length} = \text{line length}/\lambda'$$
$$= 2.5\text{ cm}/43.85\text{ cm} = 0.057\,\lambda \qquad (10)$$

Point A is rotated on a constant VSWR circle 0.057 λ toward the generator to point B. Reactance must now be added in parallel with the impedance presented at the end of the line just plotted. As parallel additions are more easily handled in admittance form, point B is converted to an admittance by rotating it one-quarter wavelength on the same constant VSWR circle. This results in point C in Figure 4. The constant conductance circle that point C lies on is noted to be 0.23. The problem now is to move along this circle towards the generator until the reciprocal of the constant resistance circle of the source impedance is intercepted. This circle does not exist on a standard Smith chart and must be constructed.

This is done by determining the radius of the constant resistance circle representing the real part of the source impedance and then constructing a circle of equal radius with its center on the real axis and its circumference tangent to the outer radius of the chart at zero resistance. When this is done the intercept with the 0.23 constant real circle is seen to lie at point D. The amount of parallel susceptance needed to move from point C to point D is:

$$B_{CP} = (B_C - B_D)(Y_o) =$$
$$(2.4 - 0.38)(24.6) = 49.72\text{ mmhos} \qquad (11)$$

This is a parallel capacitance of:

$$C_P = B_{CP}/2\pi f = 49.72/(2\pi)(470 \times 10^6) = 16.84\text{ pF} \qquad (12)$$

All that remains to finish the solution is to determine the amount of reactance necessary to reach the source at point F. To do this, it is first necessary to transpose point D, which is an admittance, to an impedance. This is accomplished by rotating point D one-quarter wavelength on a constant VSWR circle. This moves point D to point E which is on the 2.04 reactance line thus representing a series reactance of:

$$X_{CS} = (X_E) \bullet (Z_o) = (2.04) \bullet (40.65) = 82.9 \text{ ohms} \quad (13)$$

A series capacitance with this reactance is:

$$C_S = \frac{1}{(2\pi)(f)(X_{CS})} = \frac{1}{(2\pi)(470 \times 10^6)(82.9)} = 4.08 \text{ pF} \quad (14)$$

This completes the solution for the input network.

The interstage networks as well as the output network are solved in similar fashion with the following differences. In the case of the interstage networks when the imaginary term of the source impedance is other than zero, point F would be plotted at the complex conjugate of the source impedance. In the output network solution the "source" is the output load of the amplifier (50 + j0) and the "load" is the collector impedance of the output device.

	450 MHz	480 MHz	512 MHz
Power Gain	18 db	17.2 db	16 db
Bandwidth (−1 db)	5 MHz	6 MHz	8 MHz
Overall Efficiency	44.5%	46.5%	48.5%
Harmonics	All Harmonics Better Than −20 db		
Stability	Amplifier Stable under all Conditions of Drive down to V_{CC} = 5.0 volts		
Power Output	25 w	25 w	25 w
Burnout	No Damage to any Transistor with Load Open & Shorted with 0 to ± 180° Phase Angle		

FIGURE 5 – Typical Performance Specifications

Figure 5 gives details on the performance of the completed amplifier. The use of the porcelain dielectric chip capacitors for the series elements in the interstage networks was found to provide an additional 2.5 to 3.0 dB of gain over that obtained with compression trimmers as well as reducing the number of tuning adjustments necessary.

CONSTRUCTION CONSIDERATIONS

As in all RF power applications, solid emitter grounds are imperative. In microstrip amplifiers gain can be increased more than 1 dB by grounding both of the emitter leads to the bottom foil of the microstrip board by wrapping strips of copper foil thru the transistor mounting hole as shown in Figure 6.

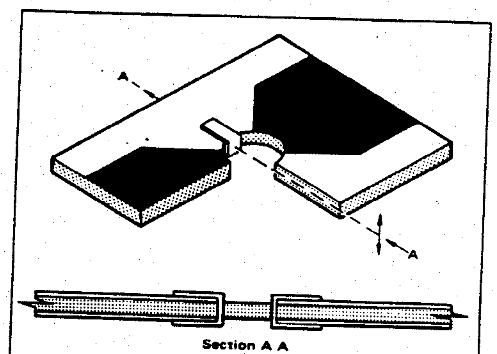


FIGURE 6 – Proper Emitter Grounding Method

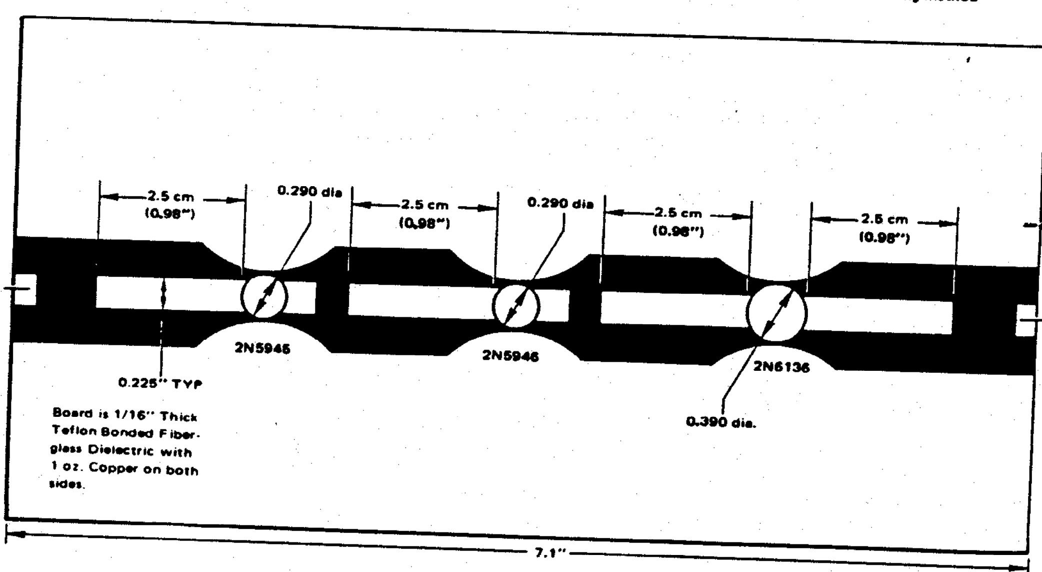


FIGURE 7a – Microstrip Board Layout

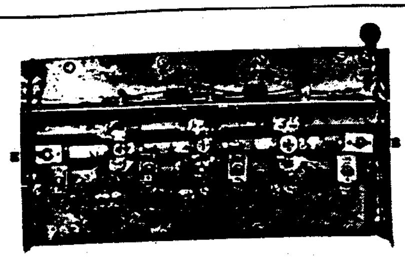


FIGURE 7b – Photograph of Amplifier

Stability under normal operating conditions is essential, however, stability should be maintained over as wide a range of supply voltage and drive levels as possible. If amplifier stability is maintained at all RF drive levels with the supply voltage reduced to between three and five volts, the designer can be practically certain that the amplifier will remain stable under all conditions of load. Maintaining stability is a key factor in protecting these transistors from damage. In a stable amplifier that has adequate heat sinking, these transistors will withstand high VSWR loads including open and shorted loads without damage. The major controlling factors in obtaining wide range stability are:

1) Mechanical layout: Good mechanical layout includes good emitter grounds (as previously described), compact layout and short ground paths.

2) Biasing: The devices are all zero biased for Class "C" operation. The use of relatively low Q base chokes with ferrite beads on the ground side will maintain good base circuit stability. In some applications, the use of a resistor in series with the ground side of the base chokes on the output and driver stages may enhance the stability. Approximate values of these resistors should be 10 ohms, 1/2 watt for the driver and 1.0 ohms, 1/2 watt for the output device. The addition of these series resistors will cause a slight loss in gain; (about 0.1 to 0.2 dB overall).

3) Collector supply feed method: The collector supply feed system is designed to provide decoupling at or near the operating frequency and a low collector load impedance at frequencies much lower than the operating frequency.

4) Heat sinking: In order to protect against burnout under all conditions of load, adequate heat-sinking must be provided. In heat sinking the device it is imperative to use a good grade of thermal compound, such as Dow-Corning 340, on the interface between the device and its heat sink.

Figure 7a shows the microstrip board layout while Figure 7b is a photo of the completed amplifier.

DEVICE HANDLING CONSIDERATIONS

Although the Motorola stripline package is a rugged assembly, some care in its handling should be observed. The most important mechanical parameter is stud-torque, specified on the data sheet at 6.5 inch-pounds maximum. This data sheet specification is an absolute maximum and should not be exceeded under any circumstances. A good limit to use in production assembly is 6 inch-pounds and if for any reason repeated assembly/dissassembly is required torque should be limited to 5 inch-pounds.

Another major precaution to observe is to avoid upward pressure on the leads near the case body. Stresses of this type can crack or dislodge the cap. This type stress sometimes occurs due to adverse tolerance build-up in dimensions when the device is mounted thru a microstrip board onto a heat sink. Many times this type of stress is applied even in the most carefully thought out designs due to solder build-up on the copper foil when a device is replaced. In device replacement care should be taken to flow all solder away from the mounting area before the stud nut is torqued. Finally, one must be sure to torque the stud nut before soldering the device leads. Refer to Motorola Application Note AN-555 for details on mounting Motorola "stripline packaged transistors.

REFERENCES

1. P. H. Smith, "Electronic Applications of the Smith Chart", McGraw-Hill, 1969.
2. H. A. Wheeler, "Transmission-Line Properties of Parallel Wide Strips by a Conformal-Mapping Approximation" IEEE Trans. Microwave Theory and Techniques Vol. MTT-12, May 1964.
3. H. A. Wheeler, "Transmission-Line Properties of Parallel Strips Separated by a Dielectric Sheet" IEEE Trans. Microwave Theory and Techniques Vol. MTT-3, March 1965.
4. H. Sobol "Extending Microwave and Technology to Microwave Equipment" Electronics, March 20, 1967.
5. Microwave Engineers Technical and Buyers Guide, Edition of the Microwave Journal, 1969.